CSCI 4974/6974 Hardware Reverse Engineering
Homework 1

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1 Assignment

Your goal is to extract a vectorized layout and full circuit schematic from the I/O cell of the XC2C32A. (You need not include the protection diodes.)

The submision deadline is March 18th, 2014. Depending on how the class is doing we may extend this deadline.

This is an experimental assignment so the difficulty may need to be adjusted. Feedback is welcome.

You may work in groups but must write up submissions individually. Use of any and all external documents and resources is permitted. You may not receive personal assistance (ex: making forum posts, in-person or online conversation) with the work from anyone who is not a student of the class.

2 Deliverables

Deliverables:

- Layered SVG file containing embedded images and vectorized layout
- Transistor-level circuit schematic, in either KiCAD EESchema or PDF format
- Gate-level circuit schematic, in either KiCAD EESchema or PDF format
- PDF document containing a brief explanation of how the circuit works, a block diagram, and a floorplan drawn over the layout showing where the major functional blocks are.

3 Data

A tar.gz file containing a series of labeled photos has been provided on the course website for your convenience. This dataset may or may not contain sufficient information for a full circuit extraction. You may also find the photo gallery

at http://siliconpr0n.org/map/xilinx/xc2c32a/ useful; it contains thousands of optical photos of the entire XC2C32A at various stages of deprocessing. If this plus the provided images are insufficient, you may take additional photos during the imaging lab.

It is known from previous RE of the device that the I/O block is controlled by several configuration bits. The configuration SRAM cells are located in the macrocell and the outputs of these cells are routed on metal 4 to the I/O cell area, then down to M2 by vias. You should find each of these configuration signals, if you can, and label them. (Some of these signals may be located in the macrocell and thus not present in the region of interest. If you believe this is the case, please state so in your writeup.)

- I/O bank voltage range selector (one bit for input and one for output, chooses low or high range; these bits are shared by all I/O cells in the bank). These bits likely select between two sets of I/O transistors which are tuned for different voltages.
- Slew rate (one bit). This bit controls how fast the outputs switch. The output driver most likely contains two transistors in parallel and this bit selects whether only one or both turn on.
- Termination (one bit). This bit determines whether the I/O pin floats when in input mode, or is connected to a pullup/keeper circuit.
- Input mode (two bits, determines whether input is connected to global routing or not)
- Schmitt trigger (one bit). Enables hysteresis on the input.
- Output enable (four bits). Known values from previous RE (not sure if active-high or active-low in the I/O cell):
  - 0 = normal output
  - 1 = open drain output (NMOS enabled, but PMOS doesn't turn on)
  - 8 = tri-state output (output buffer may be disconnected by external request)
  - 14 = drive constant zero
  - 15 = disabled (input or unused pin).

In addition to the configuration bits, which remain static during normal operation of the device, you should see three other signals connected to the I/O cell:

- Output - the value to be driven out the pad
- Output enable - if tri-state mode is selected, determines whether the output should drive or float
- Input - data from the I/O cell back to the core of the device

The Xilinx datasheets on the XC2C32A and CoolRunner-II series may also provide useful information on the high-level architecture of the I/O cell. Documents which may be relevant:

- DS090 CoolRunner-II CPLD Family Data Sheet
- DS310 XC2C32A CoolRunner-II CPLD Data Sheet
- XAPP376 Understanding the CoolRunner-II Logic Engine
- XAPP378 Using CoolRunner-II Advanced Features
- XAPP382 CoolRunner-II IO Characteristics