CSCI 4974 / 6974
Hardware Reverse Engineering

Lecture 5: Fabrication processes

QUIZ 3: CMOS layout

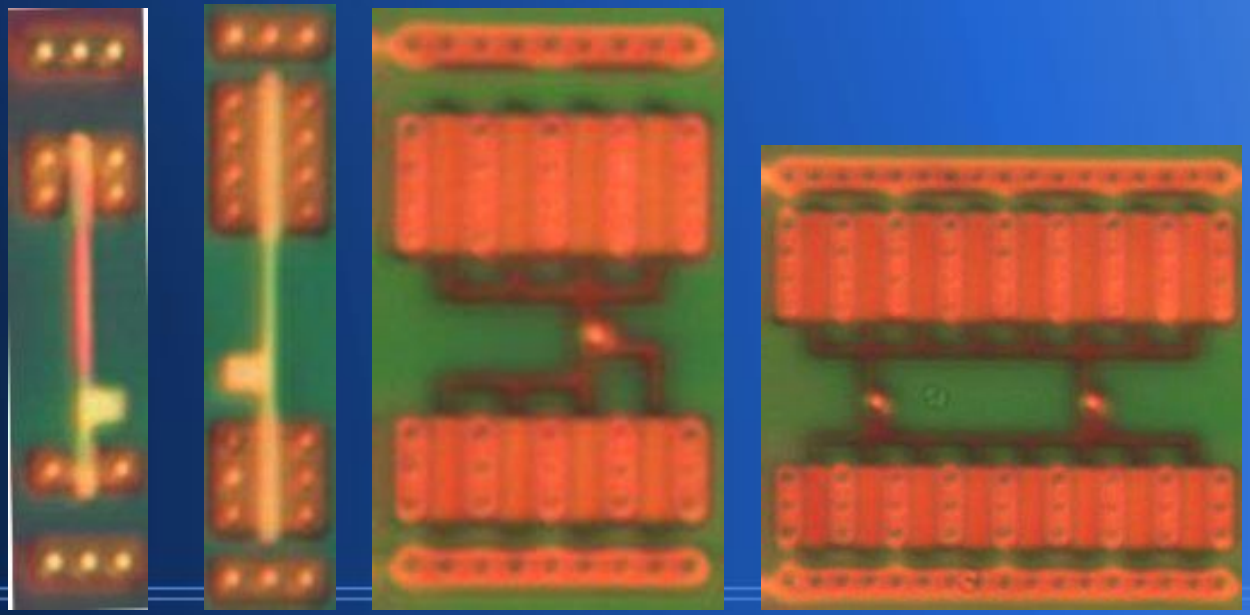
- Quiz
- Discussion

Rationale

- If you know how something is put together, you can figure out how to take it apart.
- Semiconductors are no different!

Cell naming

- Many conventions in use
- Mine is based on the Alliance cell libraries
- (gate)(numInputs)v(layout version)x(drive)
  - inv1v0x1
  - inv1v0x3
  - inv1v0x12
  - inv1v0x24



VLSI workflow - design

- Schematic entry / HDL design
- Synthesis to generic gate-level netlist
- Scan chain insertion, DFT, etc
- Technology mapping to cell library
- Placement of cells in rows
- Routing of interconnect
- Tapeout to GDS/CIF file

VLSI workflow - manufacture

- DRC and DFM checks
- CMP filler, metal slotting, etc
- SRAFs, litho optimization, double patterning
- Mask generation

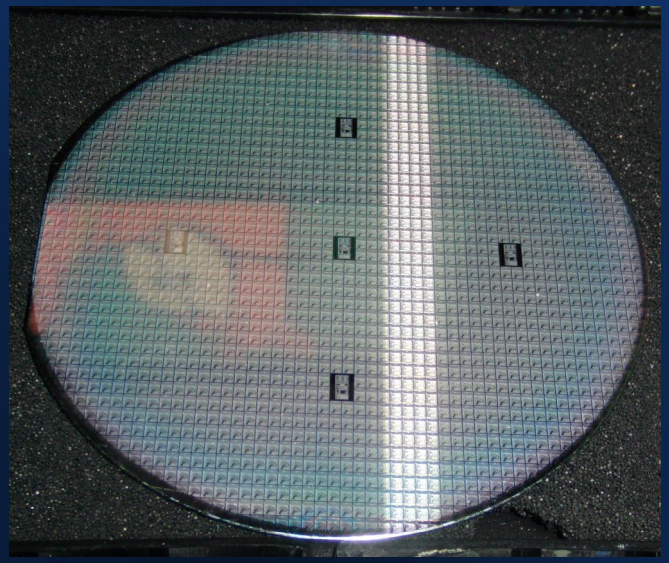
New color conventions

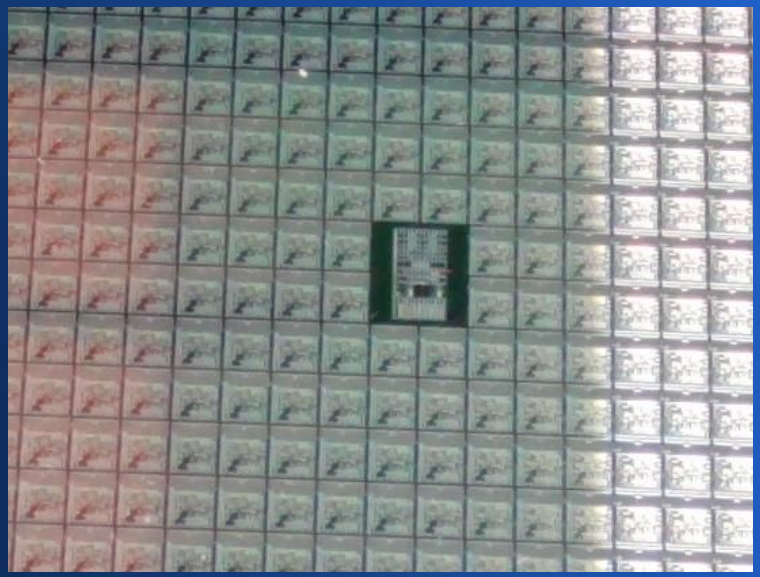
Dielectric (SiO_2)

Photoresist

Wafers vs dies

- Making one die at a time is slow and expensive
- Instead, make many at once on a wafer
- 8 and 12 inch widely used, 18 being prototyped



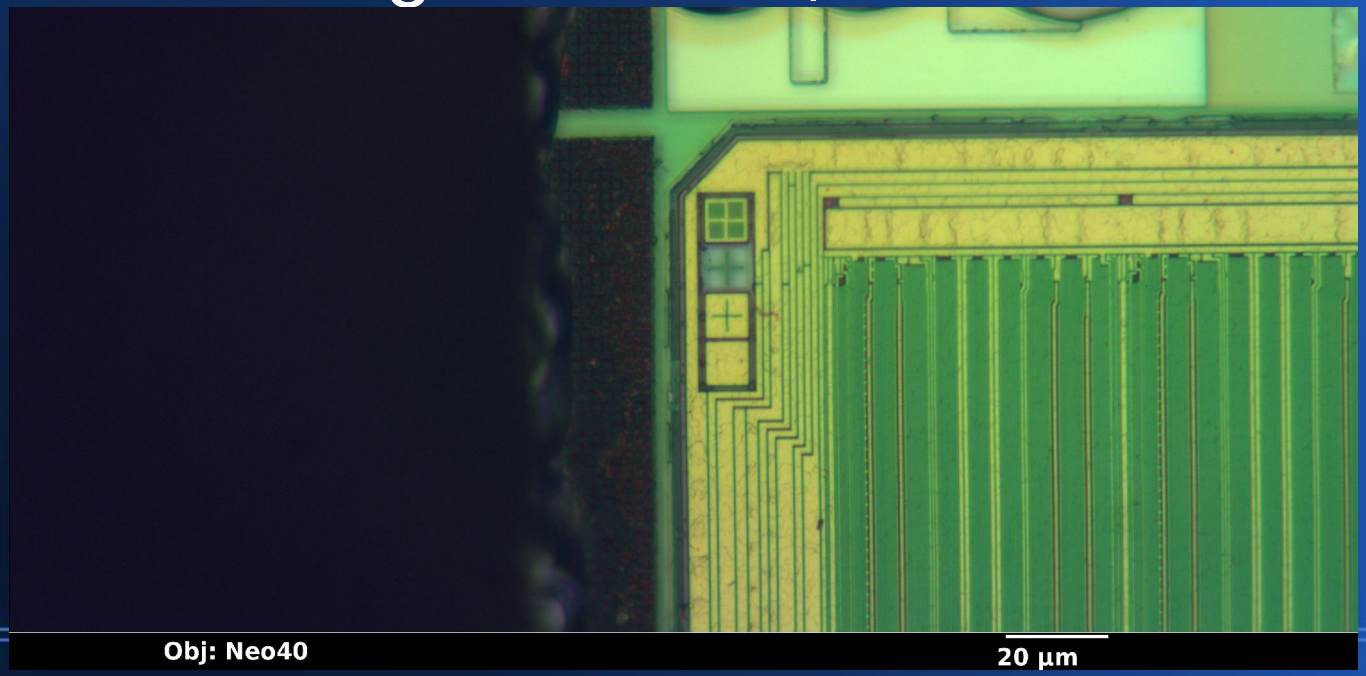


Photolithography

- IC features are too small to make mechanically
- Use optical methods instead!

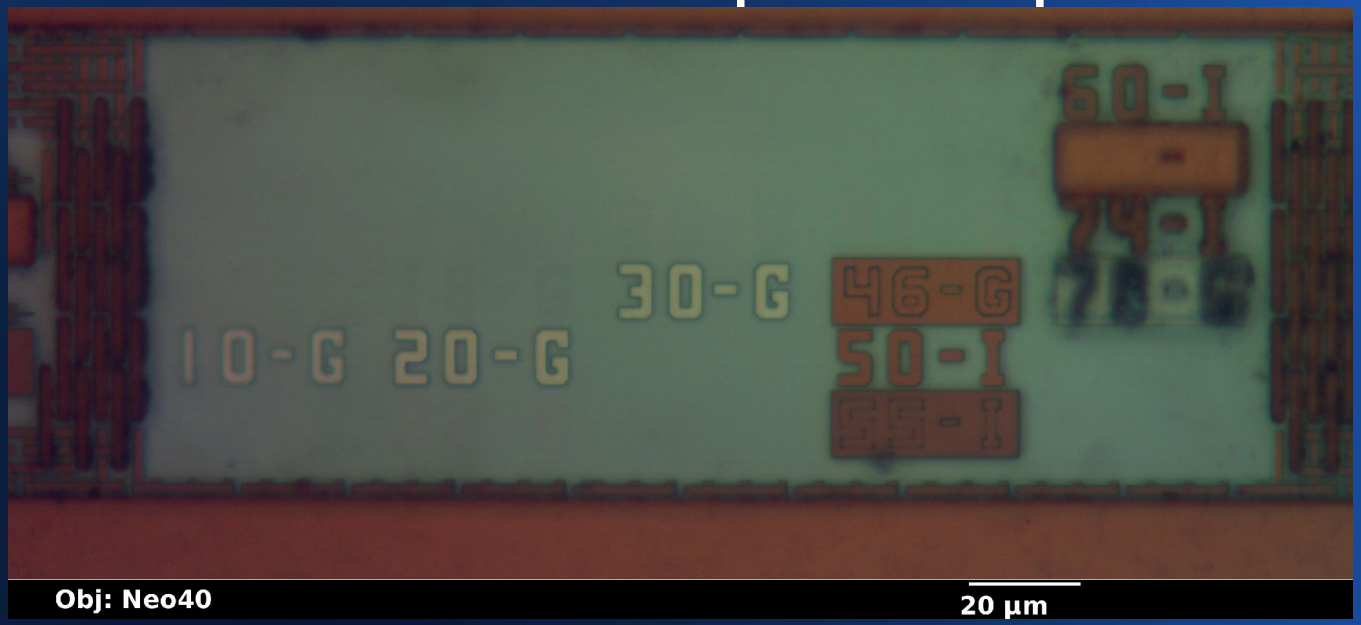
Alignment marks

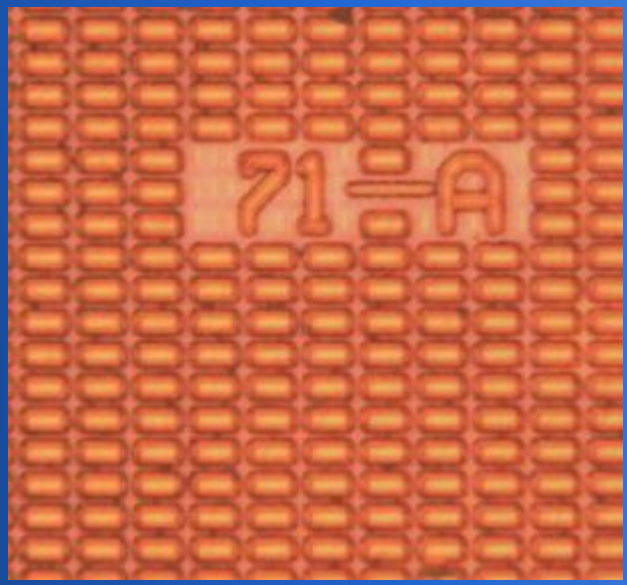
- Used to line layers up with each other
- Vary widely in appearance
- Interesting to look at, but not useful for RE



Layer numbers

- Typically take the form “number-rev”
- Allow easy ID of mask changes
- Make sure multiple samples are the same!



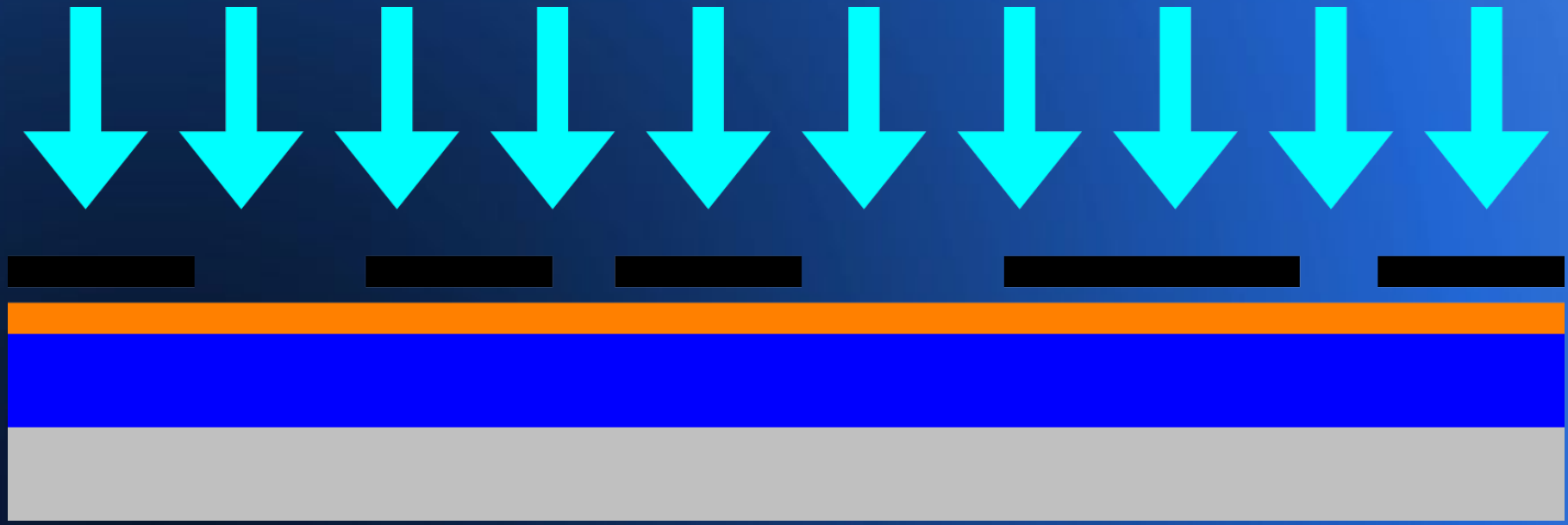


Photoresists

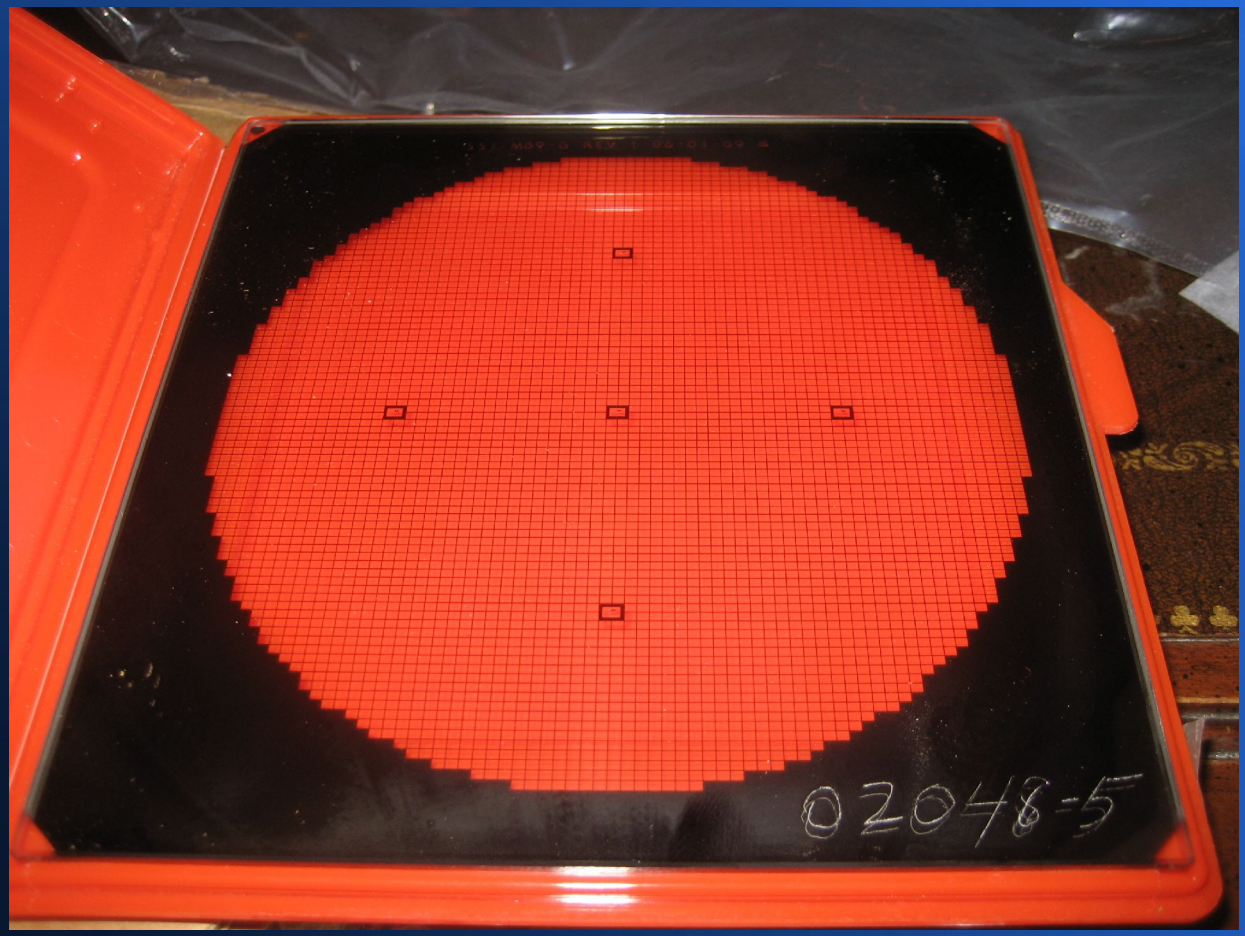
- Material which changes state when illuminated
- Insoluble -> soluble = positive acting
- Soluble -> insoluble = negative acting
- Coat on wafer
- Expose to masked light source
- Remove soluble portions in developer

Contact lithography

- Mask is 1:1 with feature
- Touching, or nearly touching, wafer

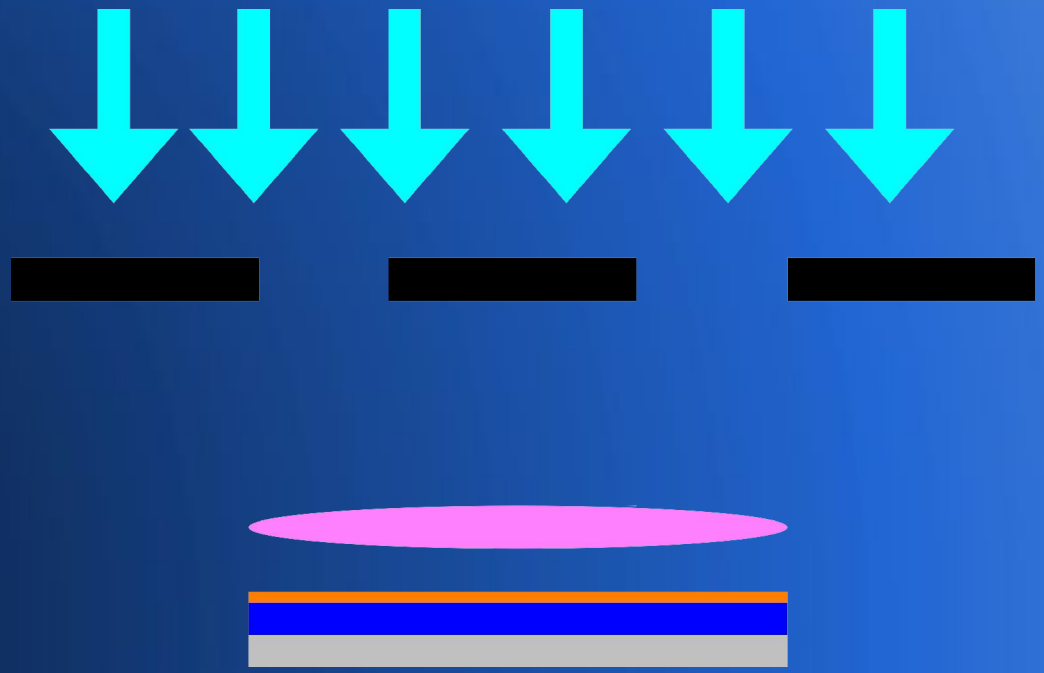


Example contact mask



Projection lithography

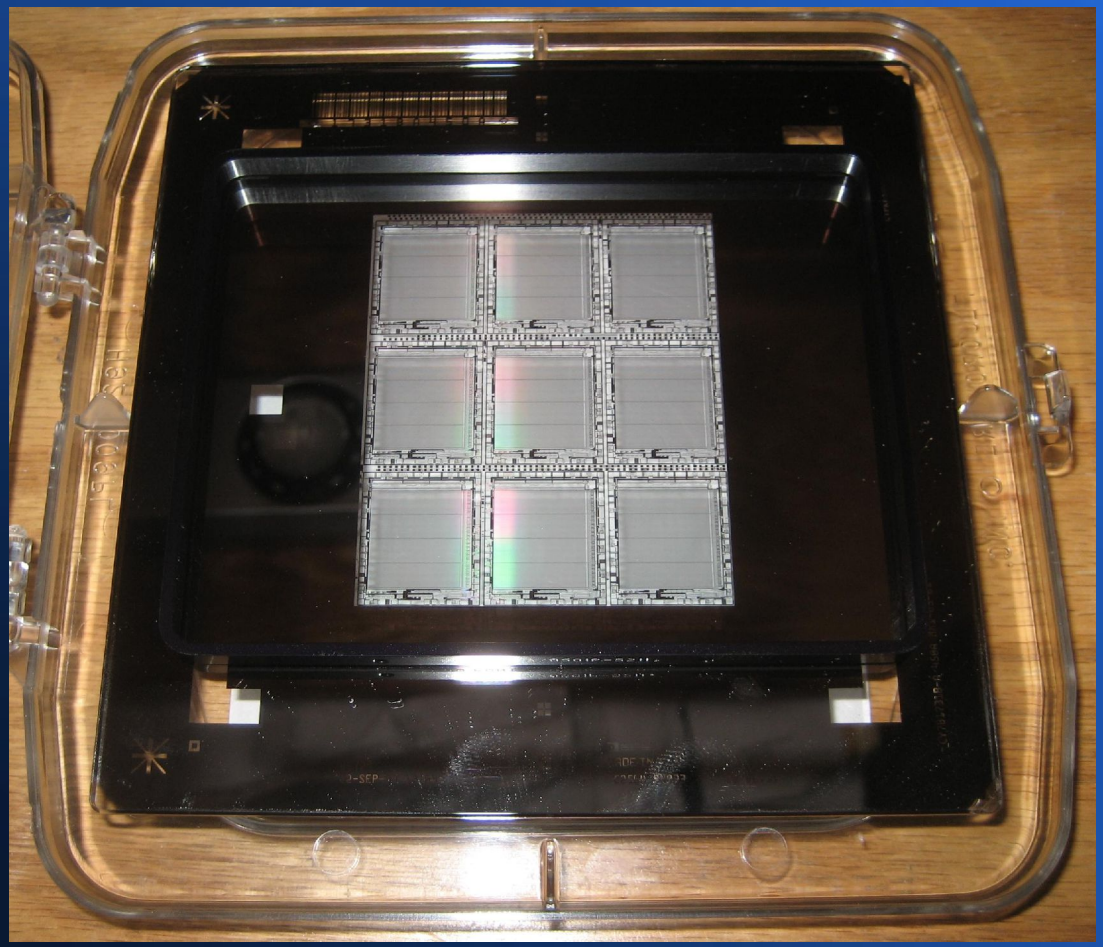
- Small features on mask are hard to make
- Mask is bigger than pattern (4:1 is common)
- Expose through lens



Steppers

- Projection masks for a full wafer would be huge
  - 4x reduction on 12” wafer = 4 feet wide!
- Lens would be massive and expensive
- Instead, mask has a few dies (or even just one)
- Step and repeat across wafer

Example stepper reticle



Direct-write lithography

- Raster-scan laser (cheap and fast, but limited resolution) or electron beam across photoresist
- Does not use a mask
  - Reduces startup costs, good for prototyping
  - Solves chicken-and-egg problem for mask fab
- Patterning time is now O(n) instead of O(1)
  - Doesn't scale well!

Multi-project wafers

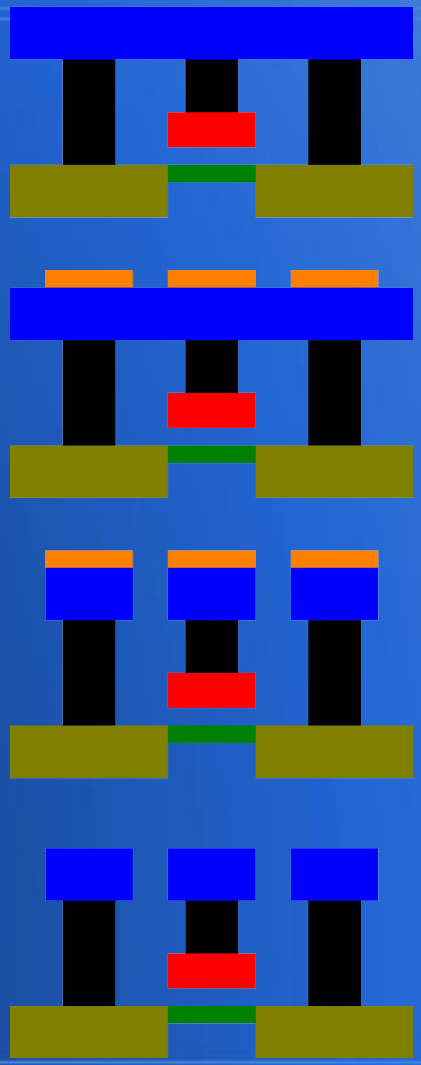
- MOSIS etc
- Also used for in-fab prototyping
- Put one die from each of many projects on a single stepper mask
- Chop them up after fab is done
- Allows many projects to share mask costs

Material patterning

- All manufacturing follows one simple algorithm
- while(product not done)
  put something on or take something off

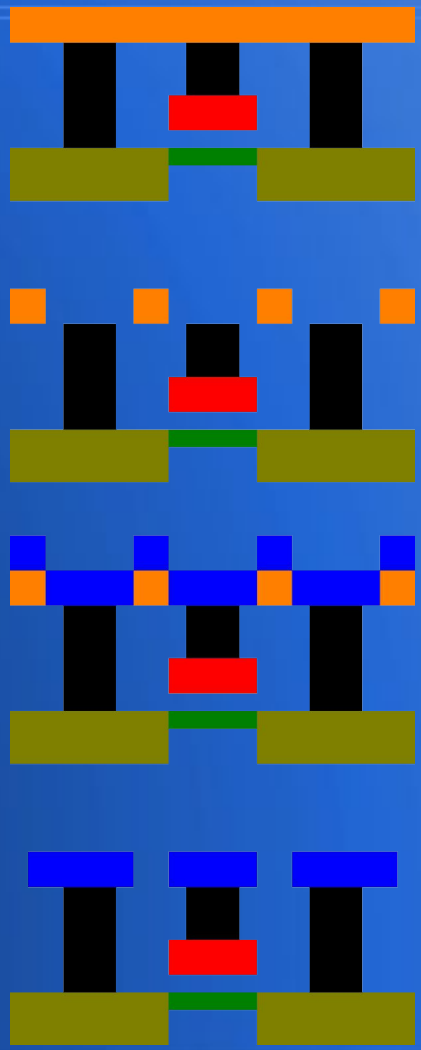
Etching

- Deposit material
- Pattern mask
- Etch material
- Strip mask



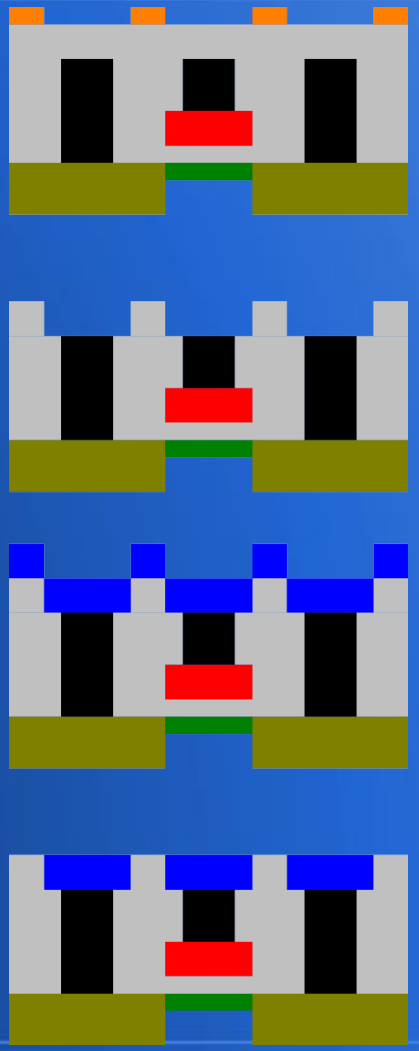
Lift-off

- Pattern mask
- Deposit material
- Remove mask and waste



Damascene

- Very similar to lift-off
- Pattern mask
- Etch dielectric
- Deposit material
- Grind/polish off extra



Dual damascene

- Same basic damascene process
- Vias and wires are formed in one step

Deposition processes

- Spin coating
- Sputtering
- Evaporation
- [PE]CVD
- Electroplating

Step coverage

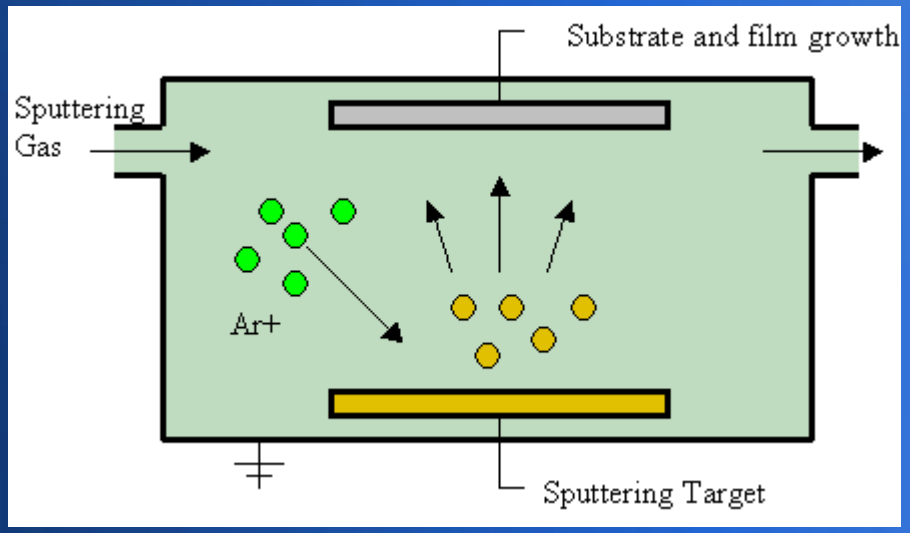
- Measure of how well a deposited film covers sharp corners
- Deeper vacuum = worse coverage (usually)
- High step coverage is usually good
- Sometimes want lower (liftoff)

Spin coating

- Mostly used for photoresists, but can be used with any soluble material
- Coat wafer with material dissolved in solvent
- Spin off extra, let dry
- Spin speed + viscosity determines thickness
- Moderate step coverage

Sputtering

- Bombard target (coating source) with plasma
- Gas ions knock off target atoms
- Gas should have similar Z to target
- Free atoms stick to wafer
- Good step coverage
- Also, reactive sputtering!



Evaporation

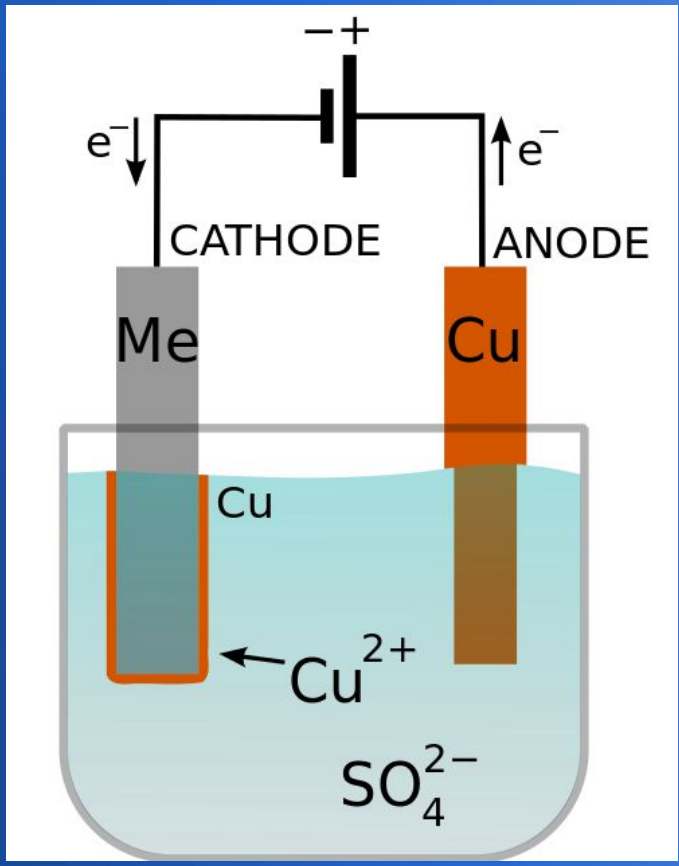
- Heat material in a tungsten dish / basket until it vaporizes
- Requires deep vacuum to avoid contamination
- Metal atoms travel in straight lines to wafer
- Can get shadowing - bad step coverage
- Can't deposit high melting point materials - what would you hold it in?
- Compounds tend to decompose

Chemical Vapor Deposition (CVD)

- Gaseous precursors flow into chamber and stick to wafer surface
- Heat/plasma decompose precursors
- Reaction products stay on wafer
- Can deposit oxides etc
- Organometallics => metals
- Good step coverage

Electroplating

- Electric field moves metal ions from solution onto sample
- Only works with metals
- Sample must be conductive
  - Sputter/evaporate seed layer
- Good step coverage

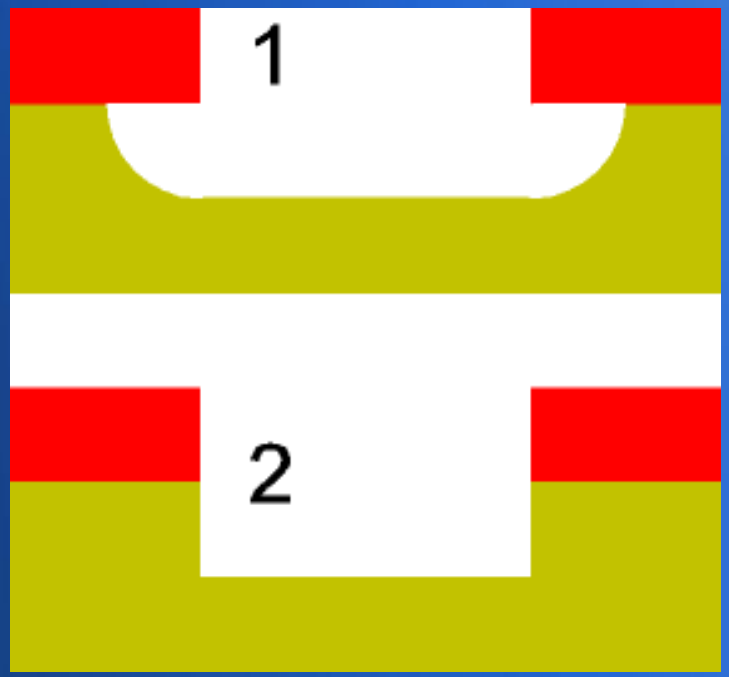


Removal processes

- Wet etching
- RIE
- CMP

Isotropic vs anisotropic etches

- Isotropic - remove material in all directions
- Anisotropic - remove preferentially in one direction
- Anisotropy is desirable in most cases



Wet etching

- Use acid or solvent to remove material
- Produces large amounts of liquid waste
- Generally fully isotropic
- Exceptions - some crystalline materials (Si + KOH)

Reactive Ion Etching (RIE)

- Fill etch chamber with low-pressure gas
- Apply RF to dissociate gas
- Ions and free radicals impact sample
  - Reaction occurs at point of impact
  - Directional motion -> etch is fairly anisotropic
- Some mechanical sputtering occurs from ions
  - Less selective than wet etch

CMP

- Chemical-Mechanical [Polishing|Planarization]
- Abrasive particles in a weakly corrosive liquid
- Press wafer against spinning polishing pad
- Chemical action weakens surface, abrasive removes reaction products

Doping processes

- Diffusion
- Ion implantation

Diffusion

- Mask areas to be left undoped
- Apply dopant source to surface of wafer, or surround it with a gaseous source
- Heat to ~1000C
- Dopant concentration, temp, time control implant depth
- Hard to get highly reproducible results

Ion implantation

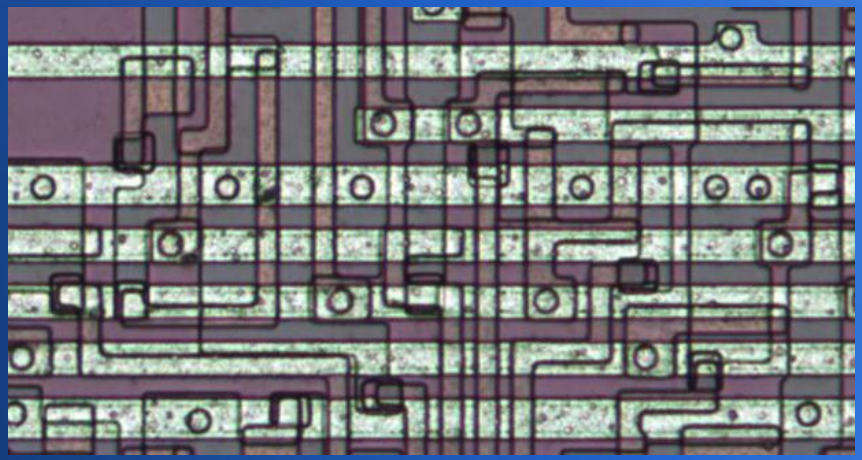
- Preferred technique for modern devices
- Mask undoped areas
- Accelerate beam of dopant ions into wafer
- Energy level controls penetration depth
- Often follow with short furnace bake to “blur” edges of implant and repair lattice defects

Other challenges

- Depth of field
- Solubility
- Wire resistance

Planarization for lithography

- Stacking many layers causes roughness
- Causes blurring of lithography
- Impacts on RE
  - Good - can see layers without deprocessing
  - Bad - gets confusing!

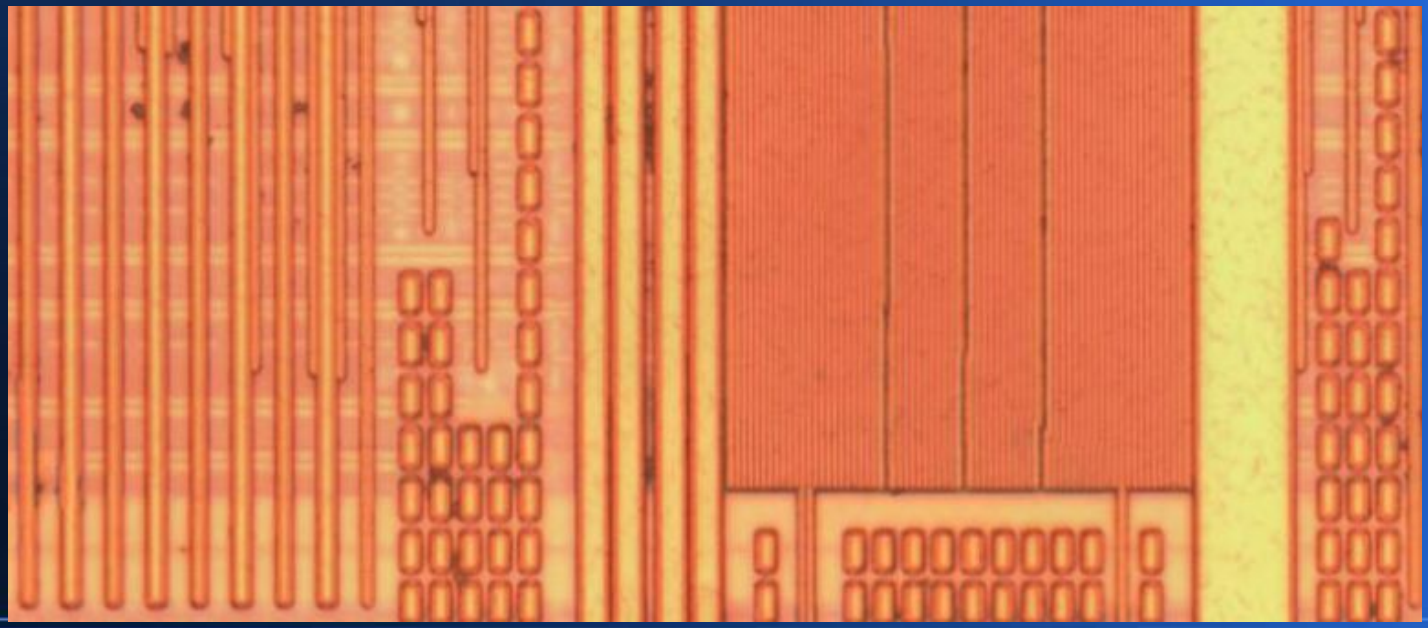


Planarization for lithography

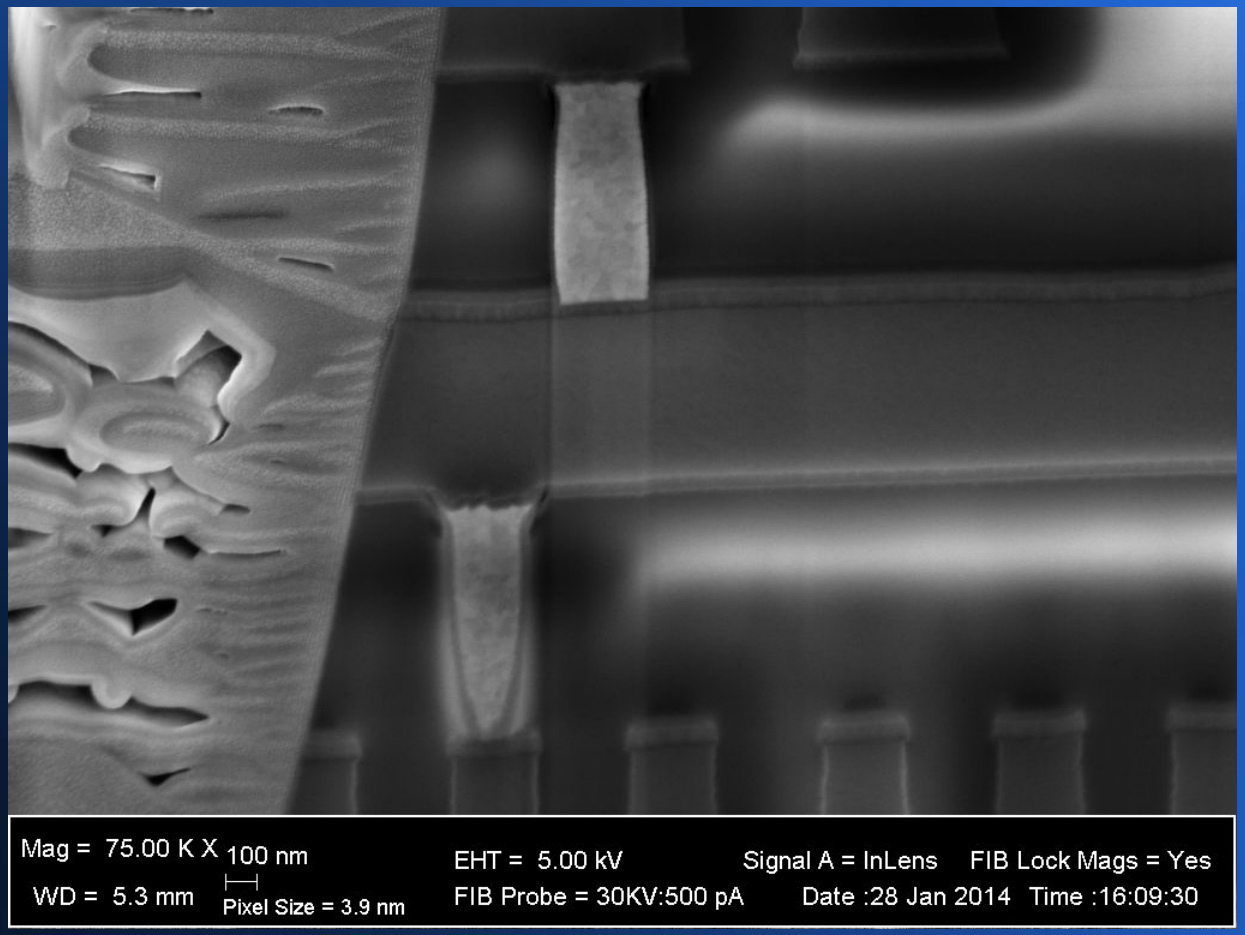
- Deposit extra ILD and CMP flat
  - Next layer is nice and smooth!
- Some fabs planarized as early as 800nm
- Most made the switch around 350
- Damascene requires planarization
- Deprocessing a must to see lower layers
- But very easy to tell what's what!

CMP filler

- Non-uniform metal density causes sagging
- Fill empty spaces with dummy metal
- Filler patterns sometimes can ID tools/vendors!



Layer sagging over via

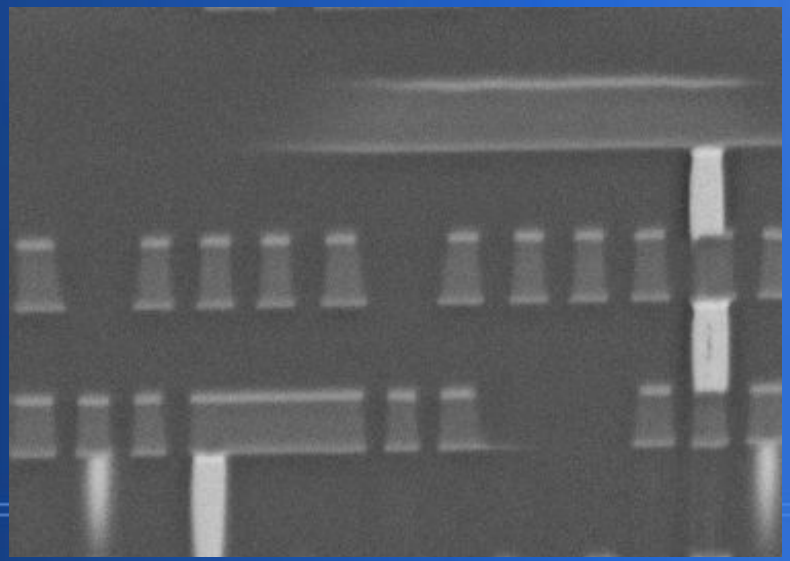


Copper metalization

- Copper is a better conductor than aluminum
- Can't use RIE - no gaseous compounds
- Need to use damascene patterning
  - Always planarized
- Barrier layer required

Adhesion / barrier layers

- Copper dissolves into ILD, reaches active layer, and acts as an unwanted dopant
- Lots of metals don't stick well to SiO_2
- Use thin layer of something else
- Aluminum - top and bottom
- Copper - all sides

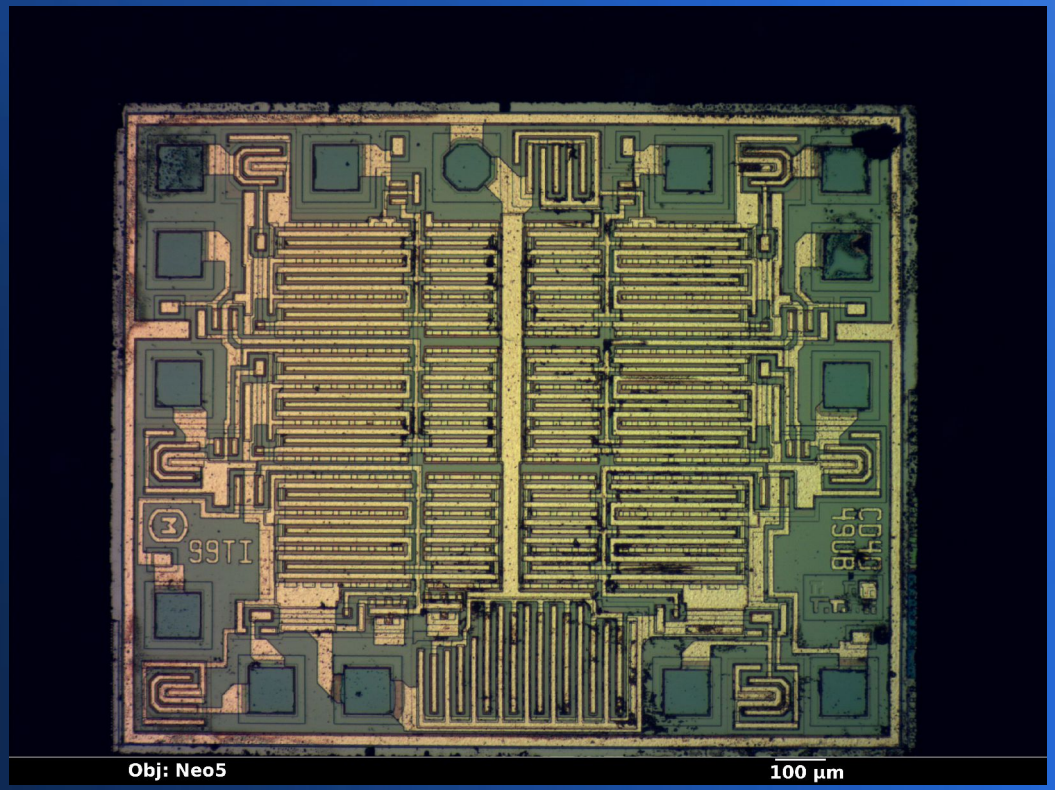


Technology nodes

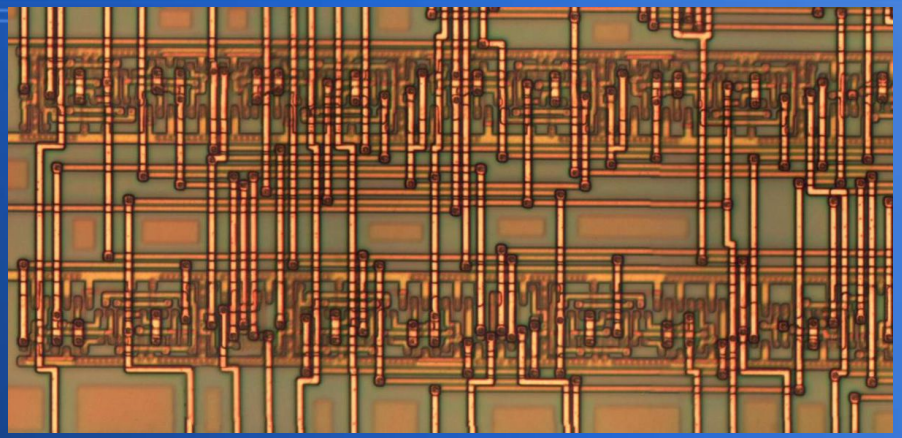
- Semiconductor technology has advanced massively over its fairly short history
- Knowing the target's process node helps estimate difficulty of REing

Huge (>2 µm)

- Generally one metal, one poly layer
- Discrete logic
- Intel 4004
- Hand layout
- Nonplanarized



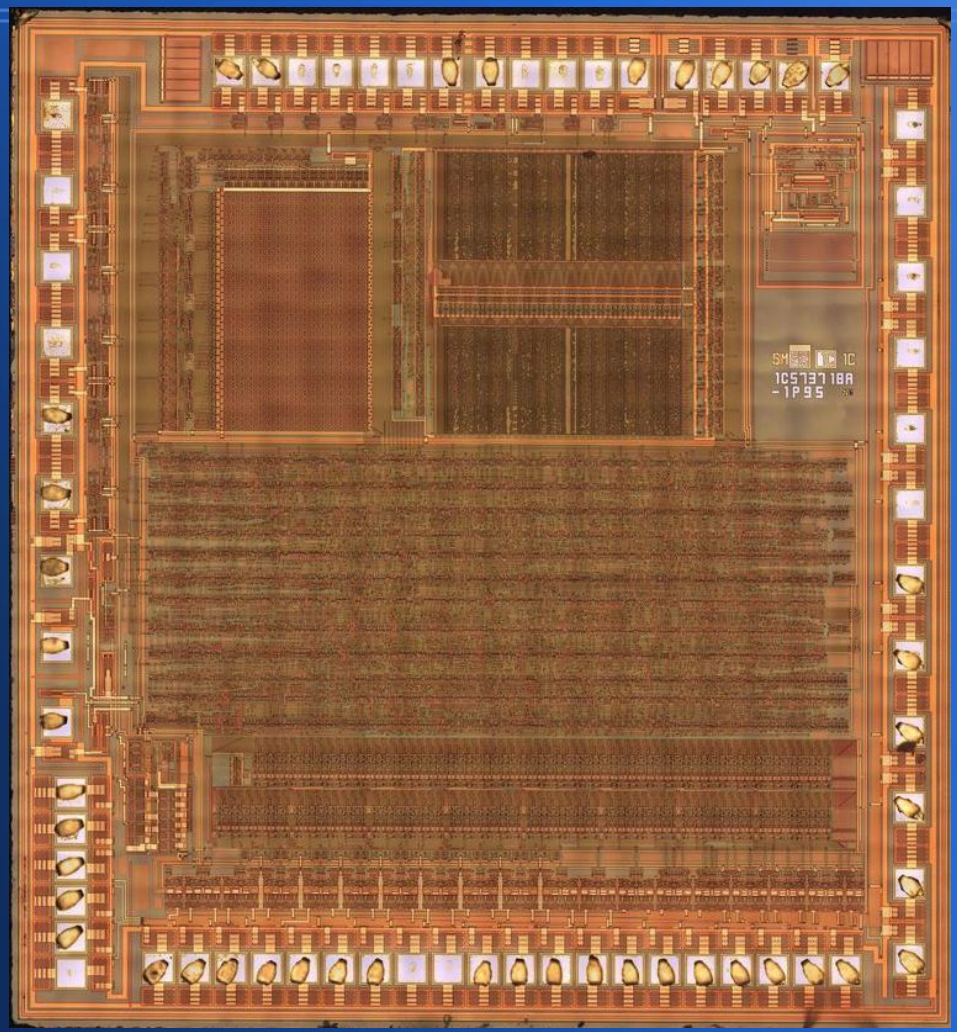
2 µm - 500 nm



- Usually 2 metal layers
- Nonplanarized
- Often use standard cells
- Horizontal signal routing between cells
- Vertical signal routing on top of cells
- Power on rings around chip and both layers
- Almost always aluminum

1 µm - die overview

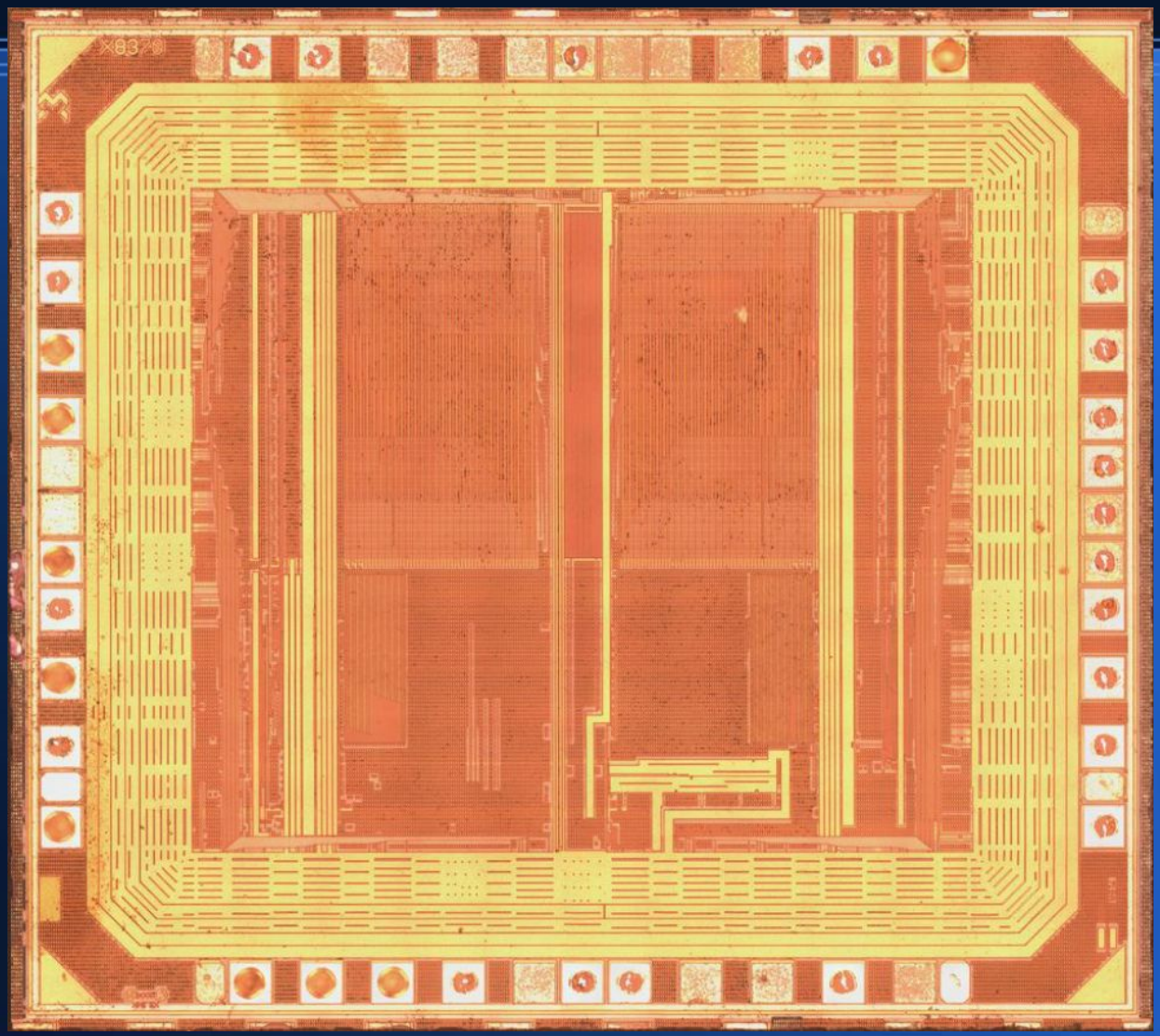
- All structure visible on top layer



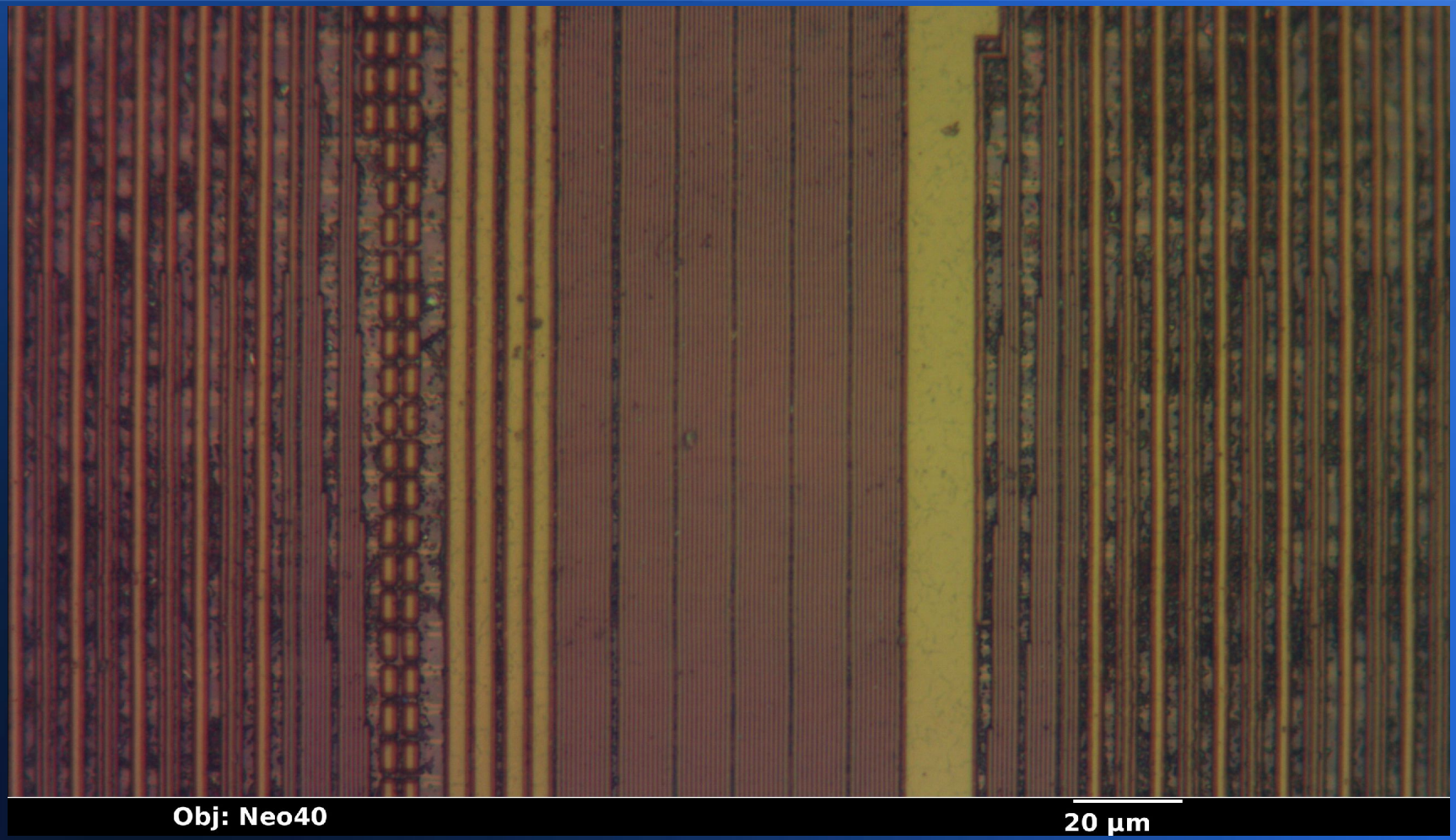
350 - 180 nm

- 3-5 metal layers
- Almost always planarized
- Power on rings around chip
- Some power routing on top layer
- Signals usually still all the way up to top layer
- Usually aluminum, some copper at 180 nm
- Some structure visible from top layer

180 nm - die overview



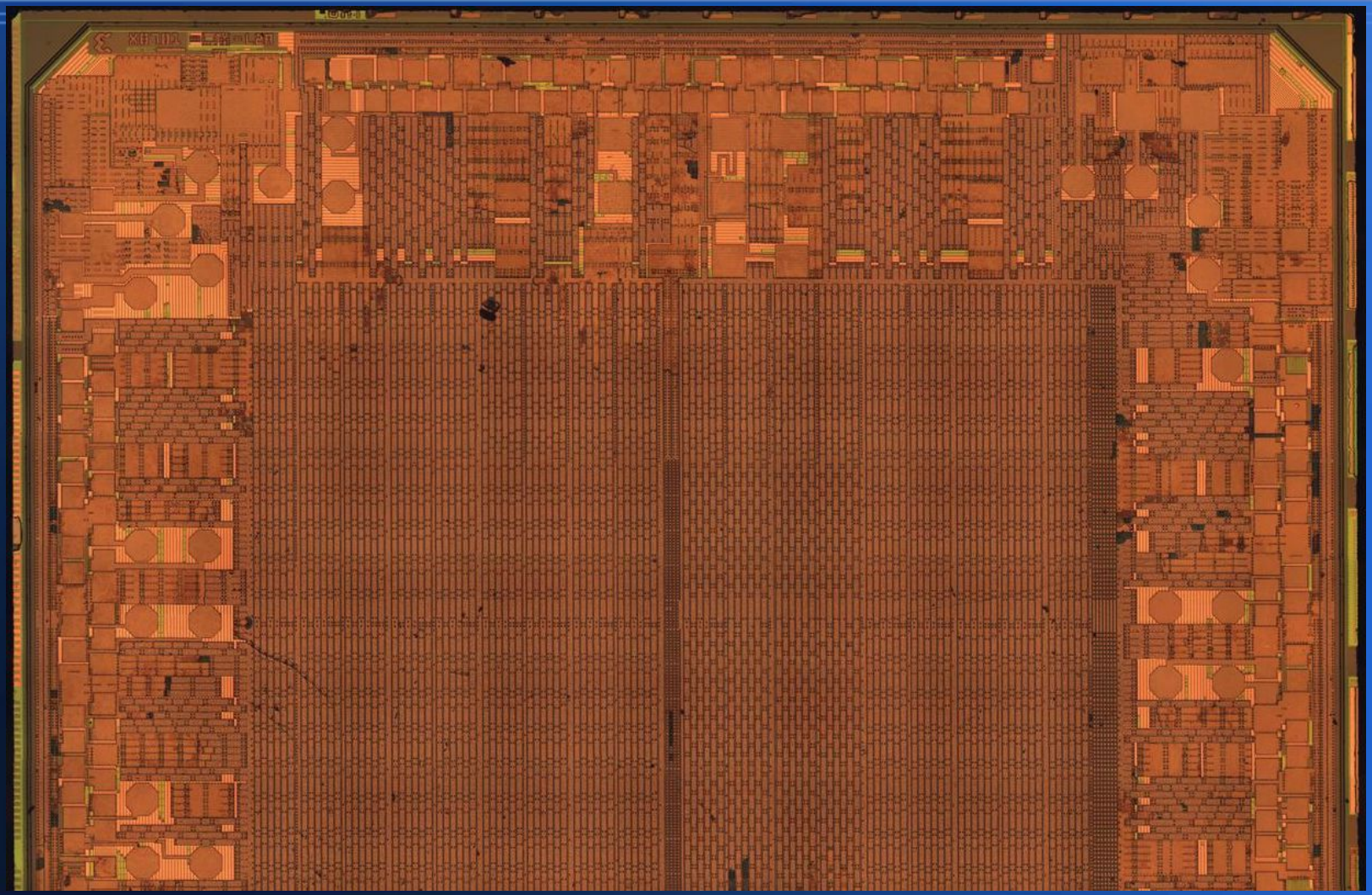
180 nm - closeup of M4



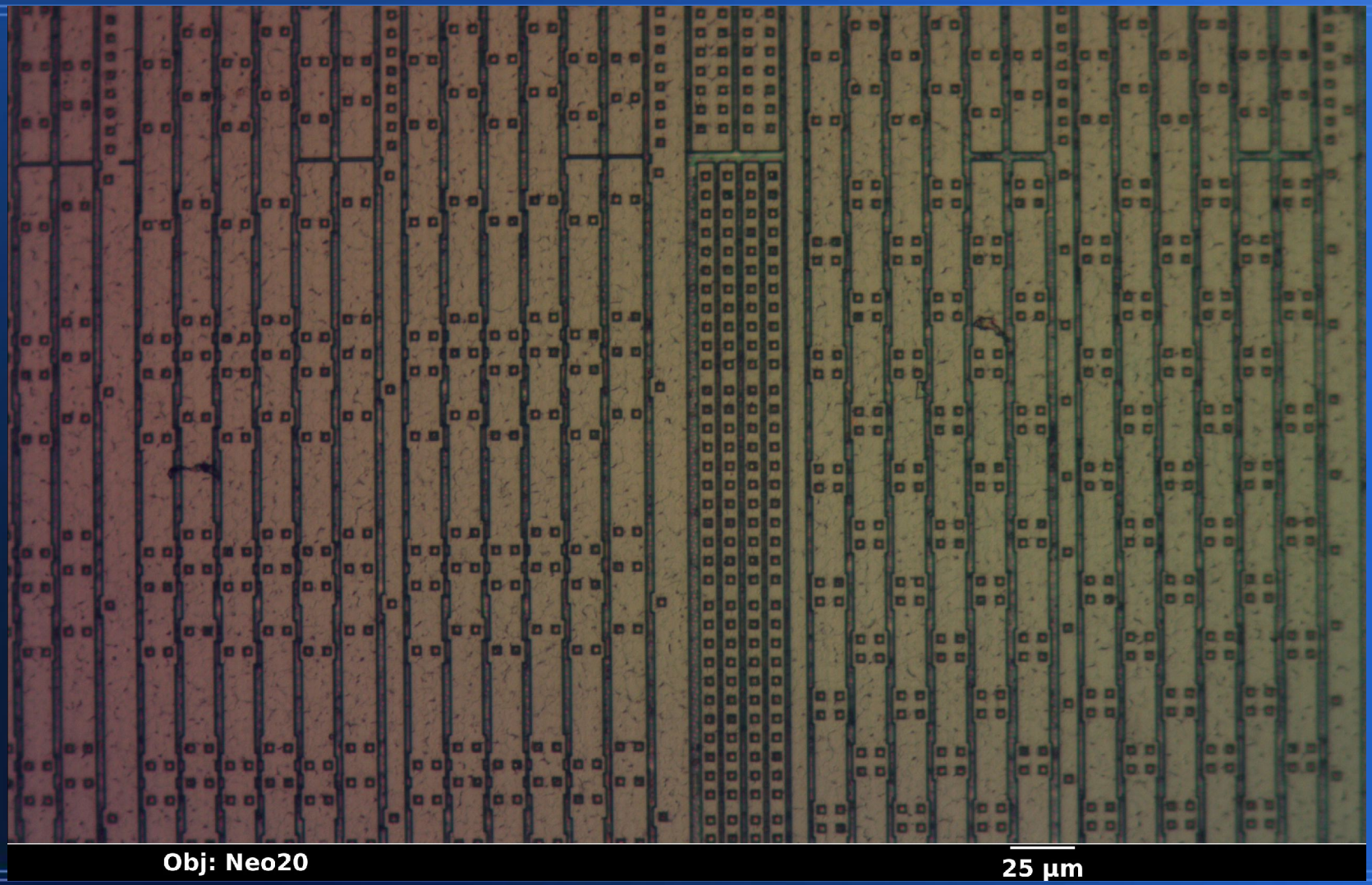
<= 130 nm

- 7 or more layers
- Always planarized
- Almost always Cu (top layer sometimes Al)
- Top layer is power exclusively, often *larger* pitches than midrange nodes
- Almost no internal structure visible from top

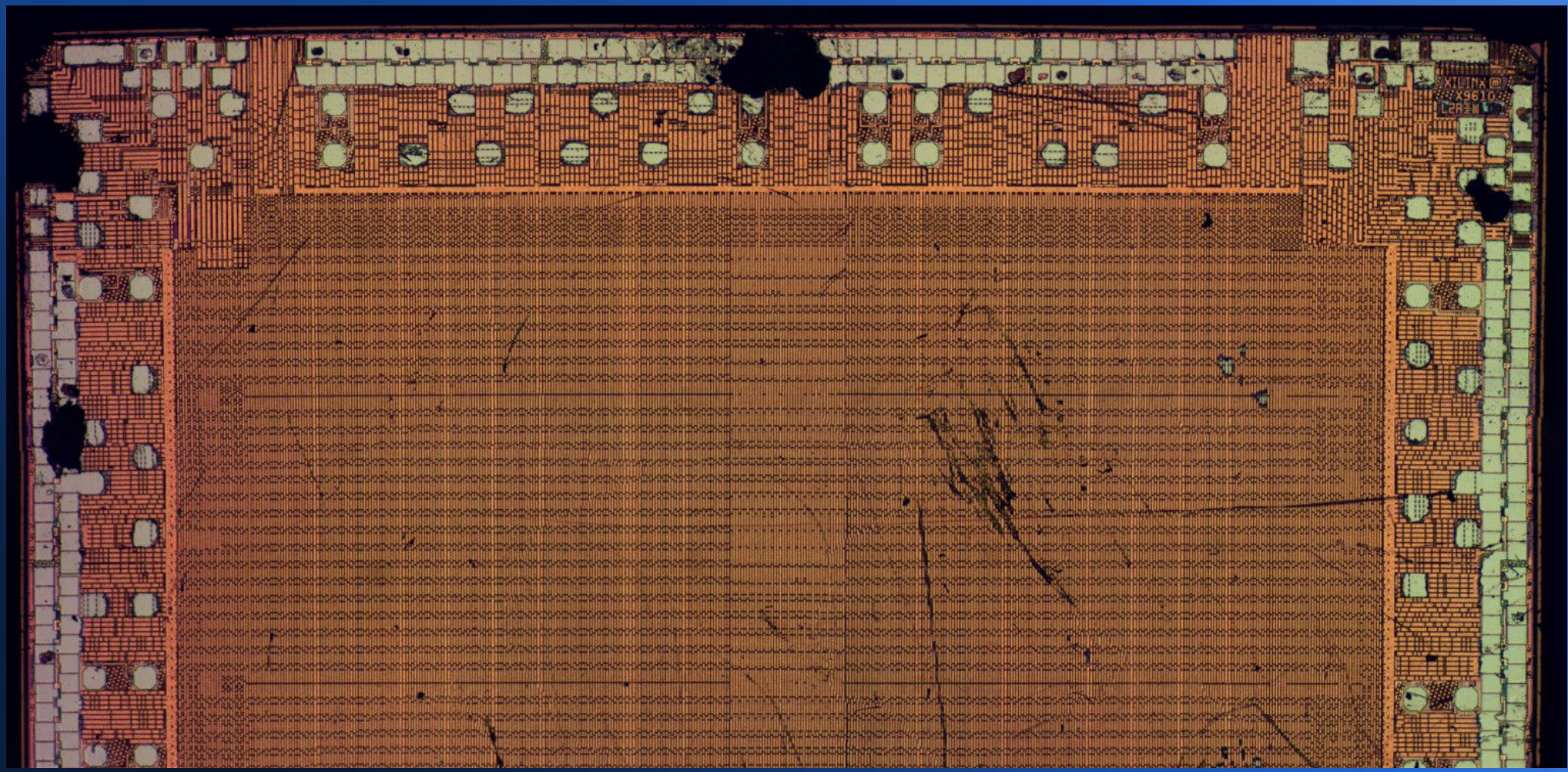
90 nm - die overview



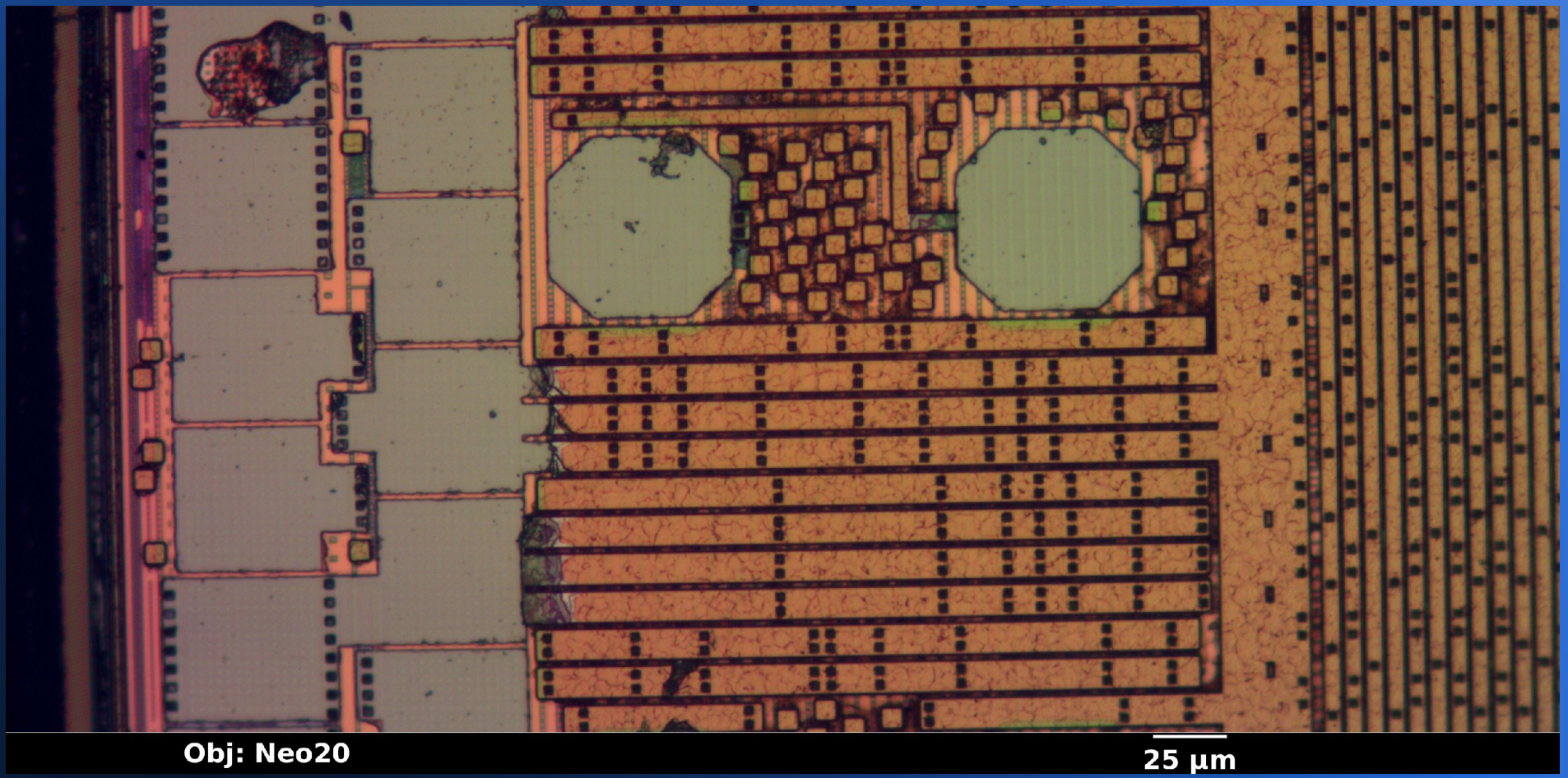
90 nm - closeup of M8



45 nm - die overview



45 nm - closeup of M9



Questions?

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