CSCI 4974 / 6974
Hardware Reverse Engineering

Lecture 4: CMOS layout

Inkscape

- Vector graphics editor
- Very useful for visualizing VLSI layout
- Demo
- Download today's examples

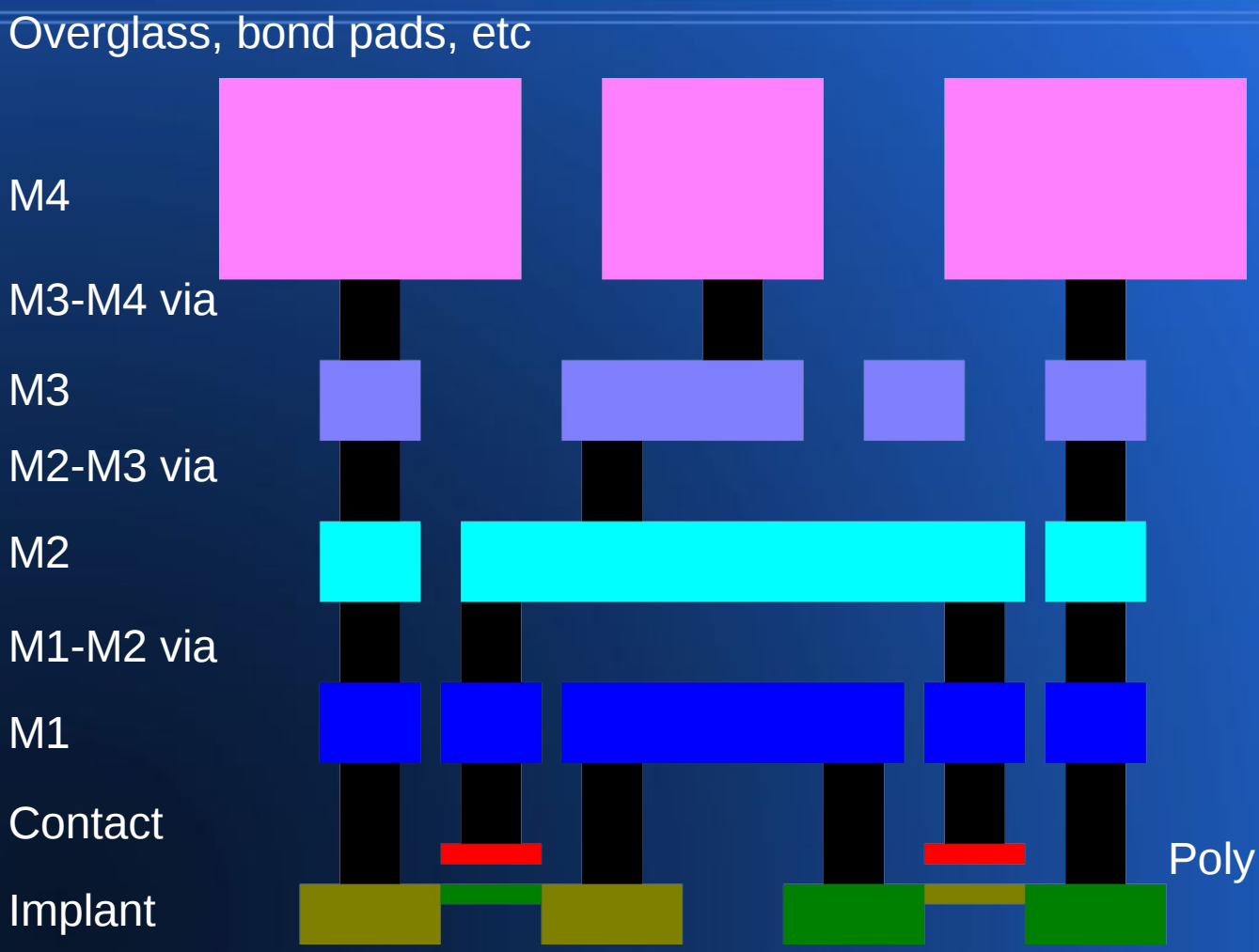
Materials

- Silicon
  - Undoped
  - P-type
  - N-type
  - Polycrystalline
- Insulators
  - Usually SiO_2
  - Sometimes low-k
- Metal
  - Multiple layers
  - Numbered in order

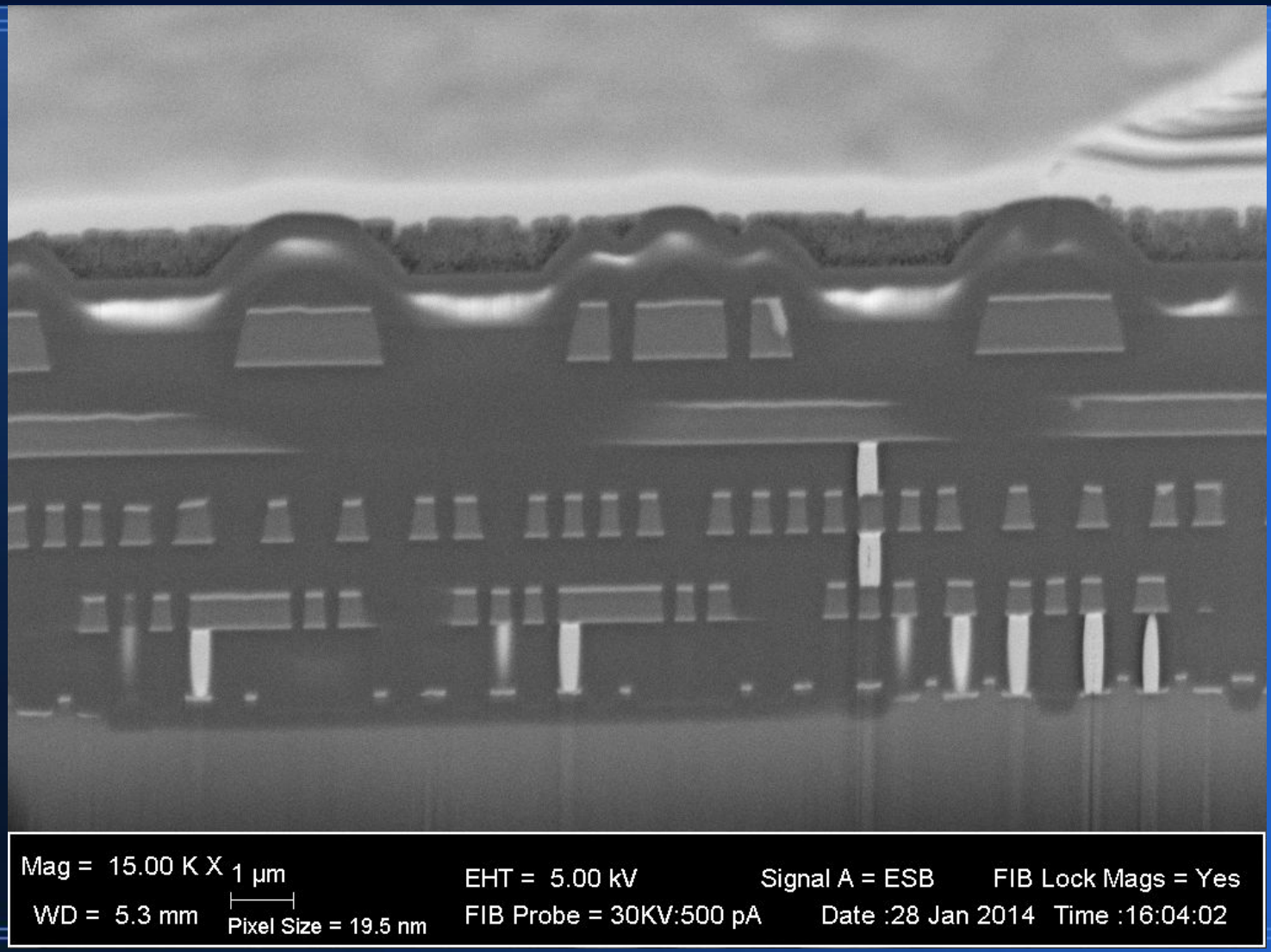
Color-coding convention

- Based on scheme used in Mead & Conway
- Extended for multilevel metallization

Schematic cross section

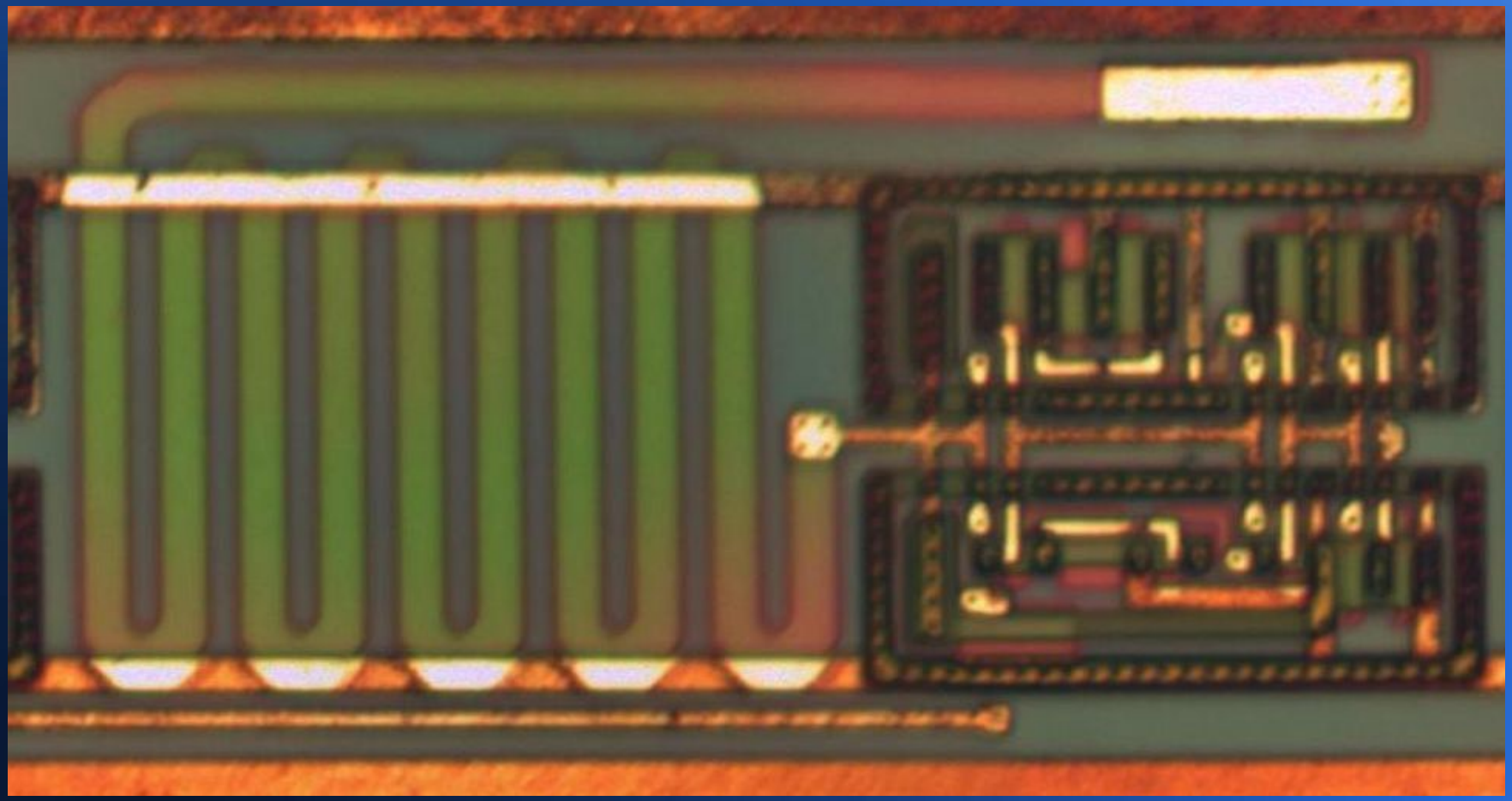


Actual cross section (XC2C32A)



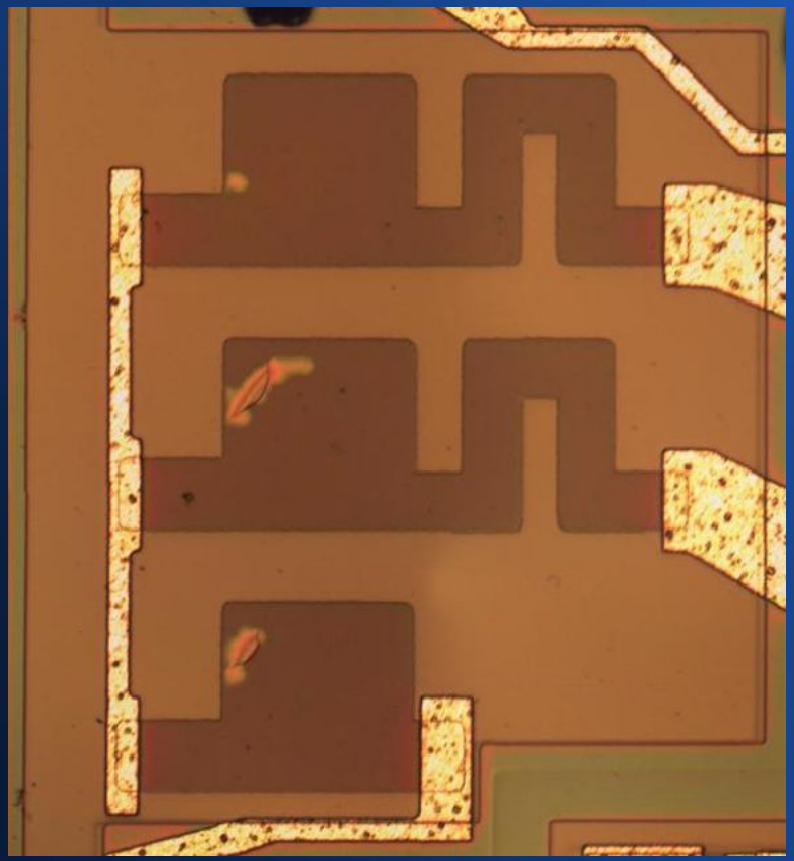
Poly resistor

Actual poly resistor



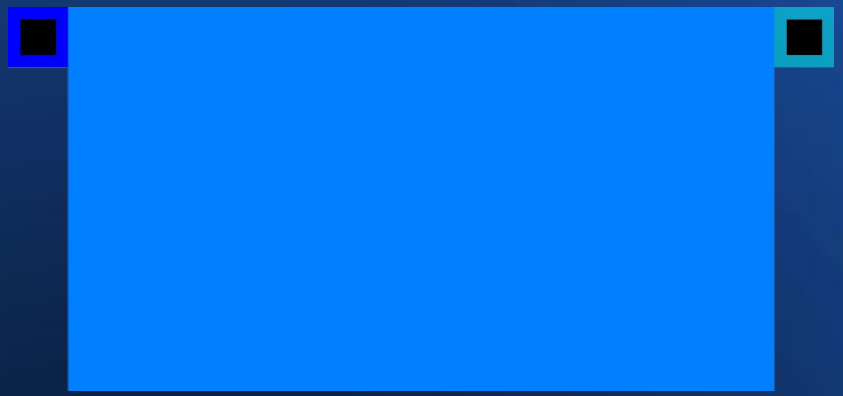
Laser-trimmed film resistor

- Typically only seen in precision analog

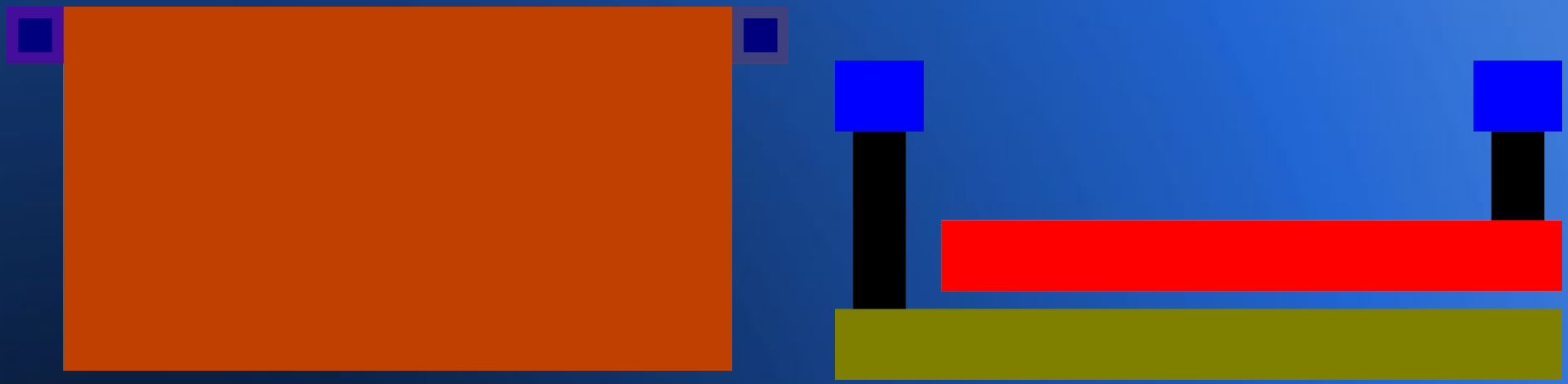


MIM capacitor

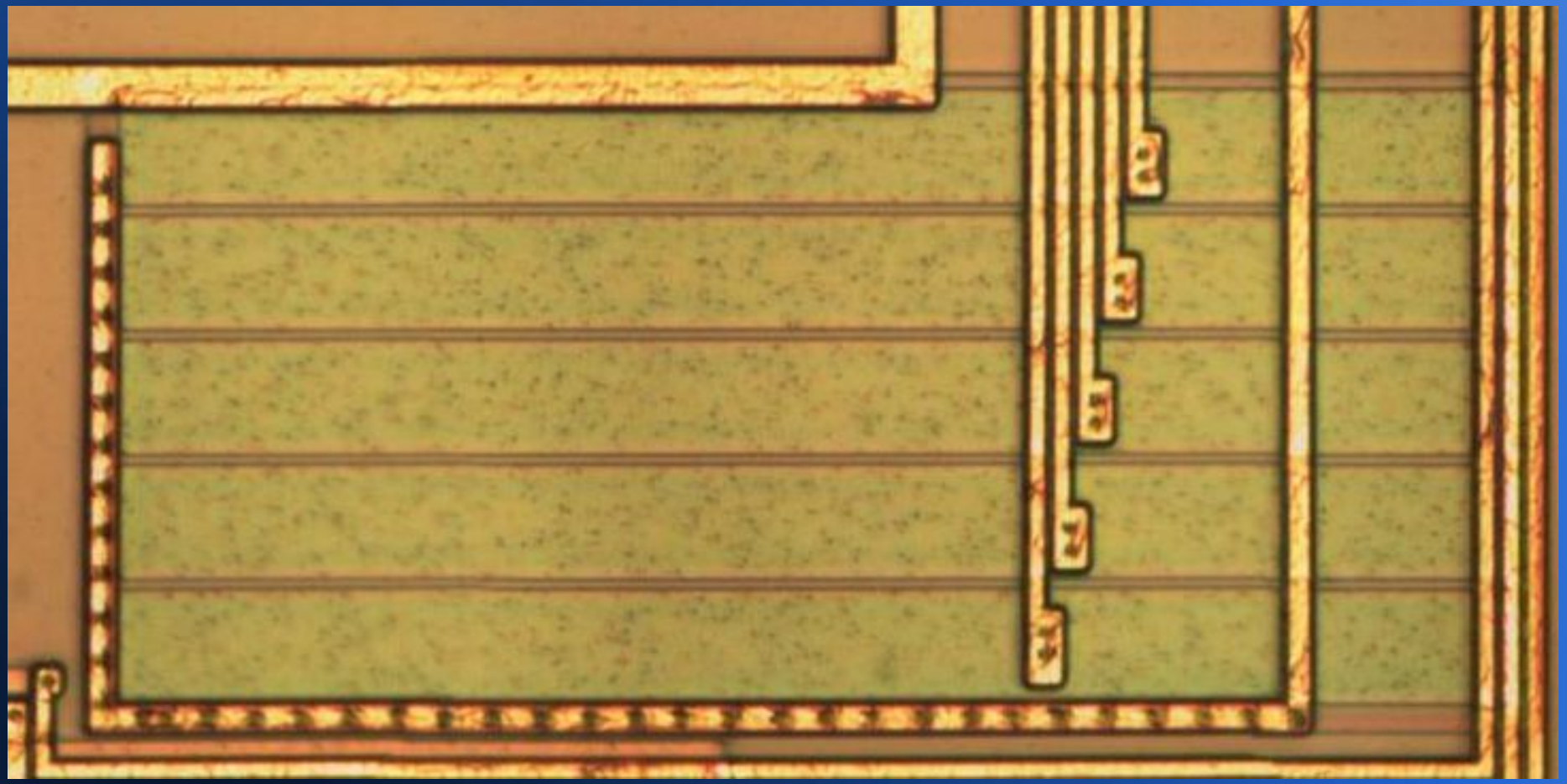
- Metal-Insulator-Metal



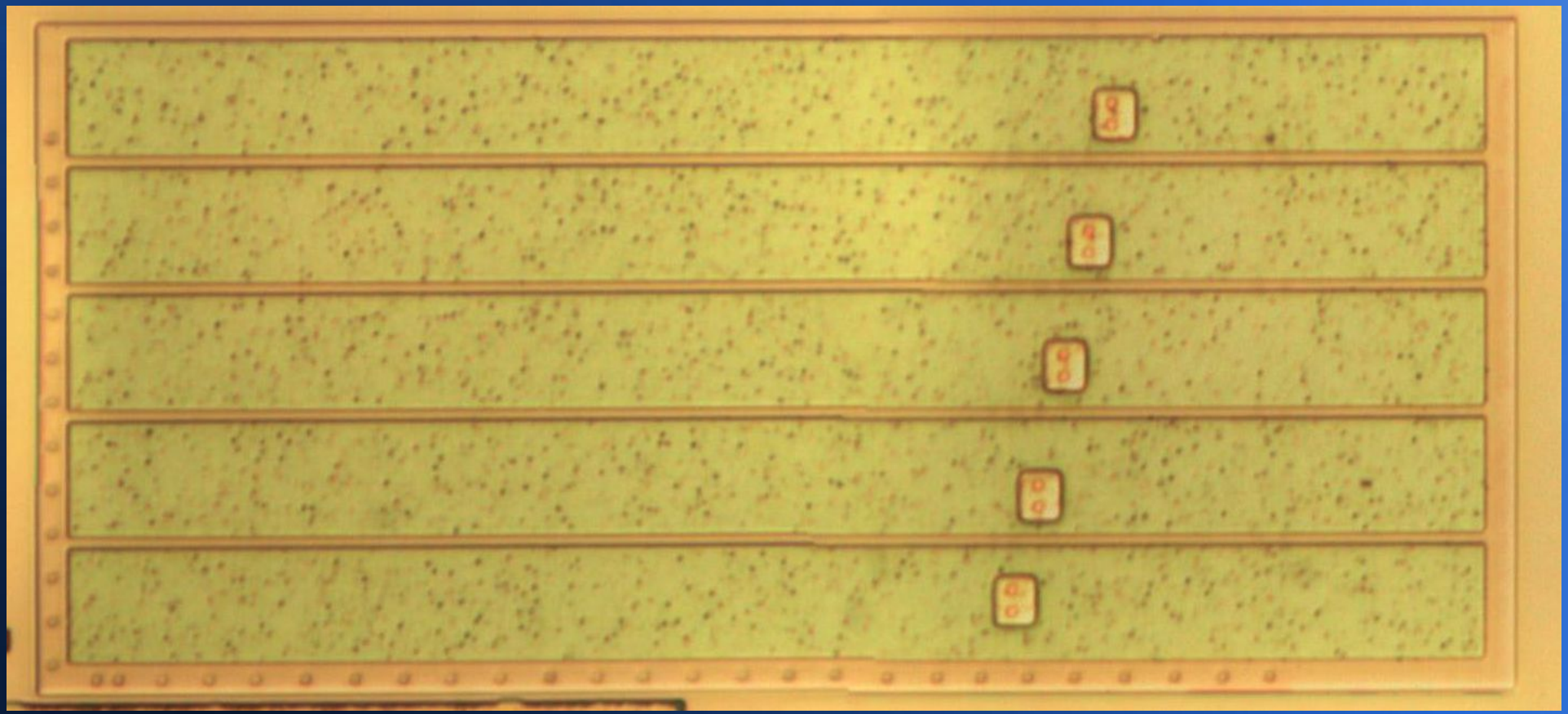
Poly (MOS) capacitor



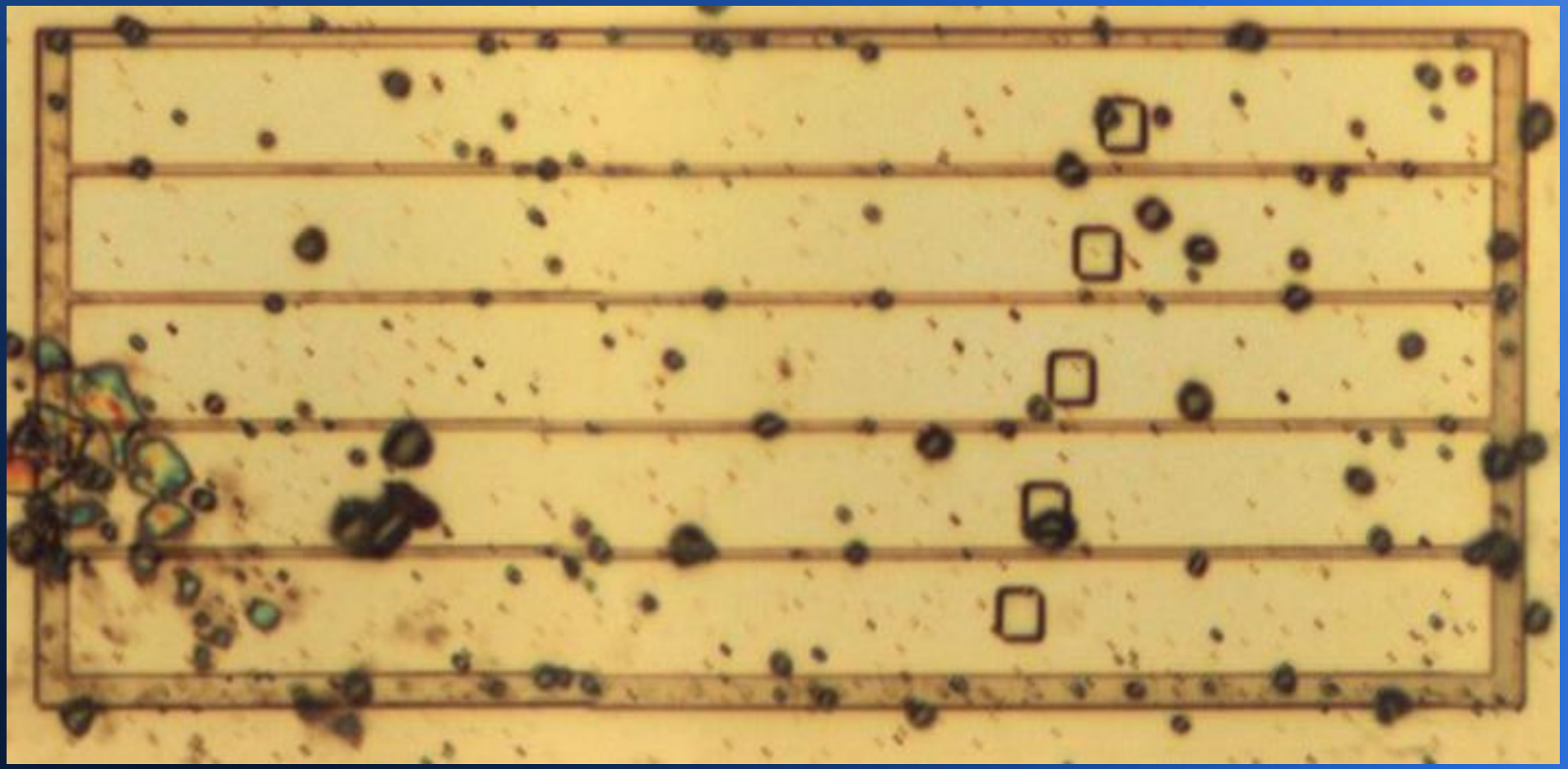
Actual MOS cap (24C02): M1



Actual MOS cap: Poly



Actual MOS cap: Implant



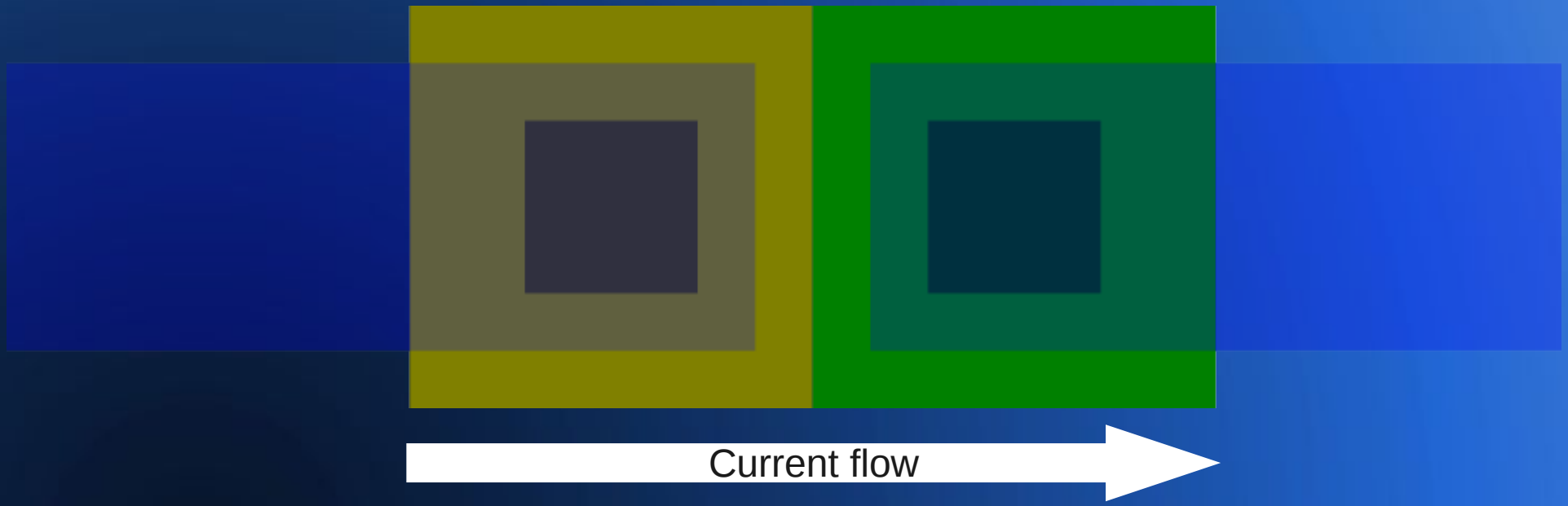
Semiconductor doping

- Semiconductors have few free charge carriers
- Add trace amounts of materials with
  - Extra valence electrons (N-type): P, As
  - Holes in the shell (P-type): B
- Greatly increases conductivity

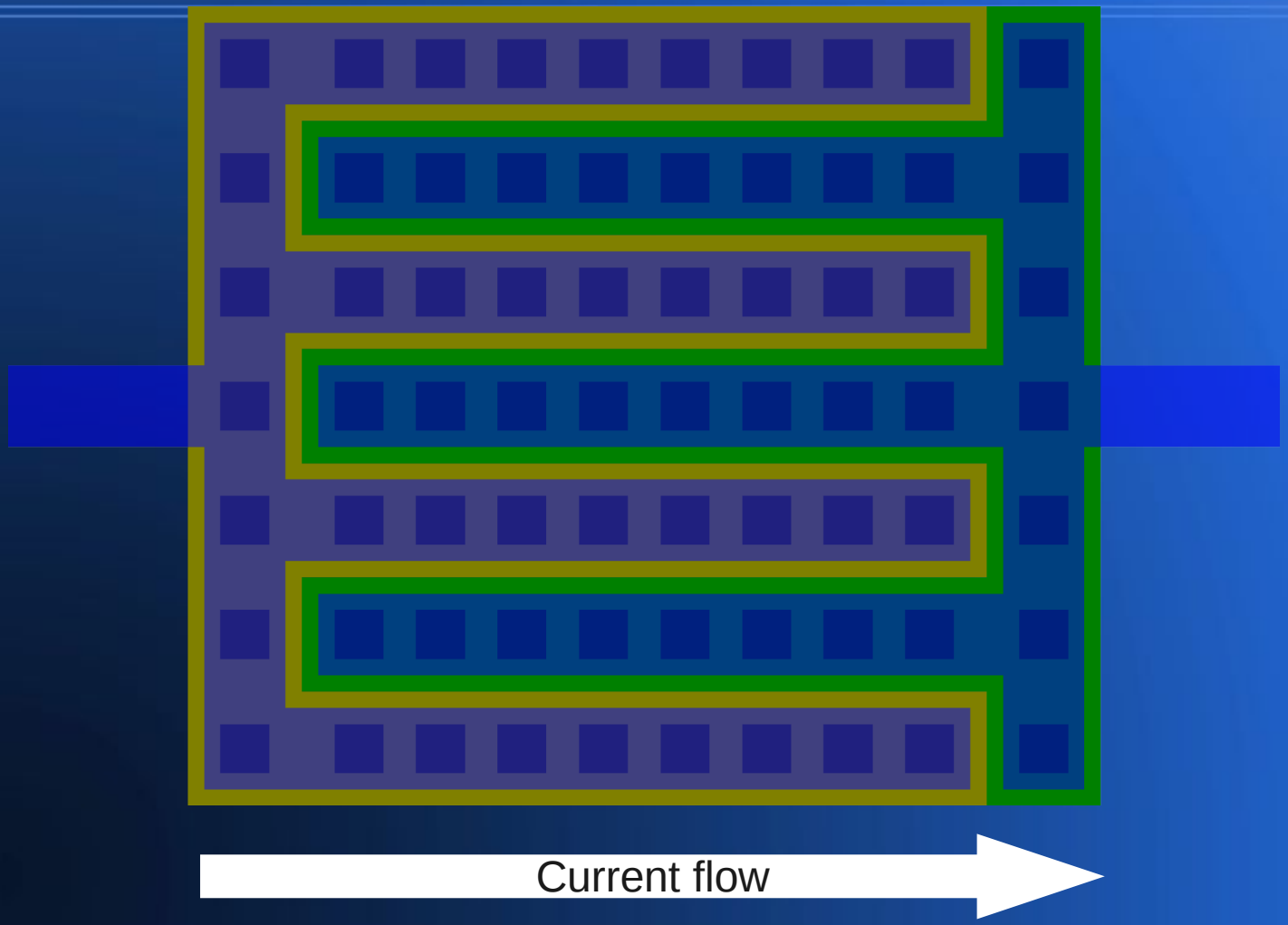
P-N junctions

- Forward bias (P-type higher voltage)
  - Charges pulled across junction
  - Current flows freely
- Reverse bias (P-type lower)
  - Charges pulled away from junction
  - No current flows

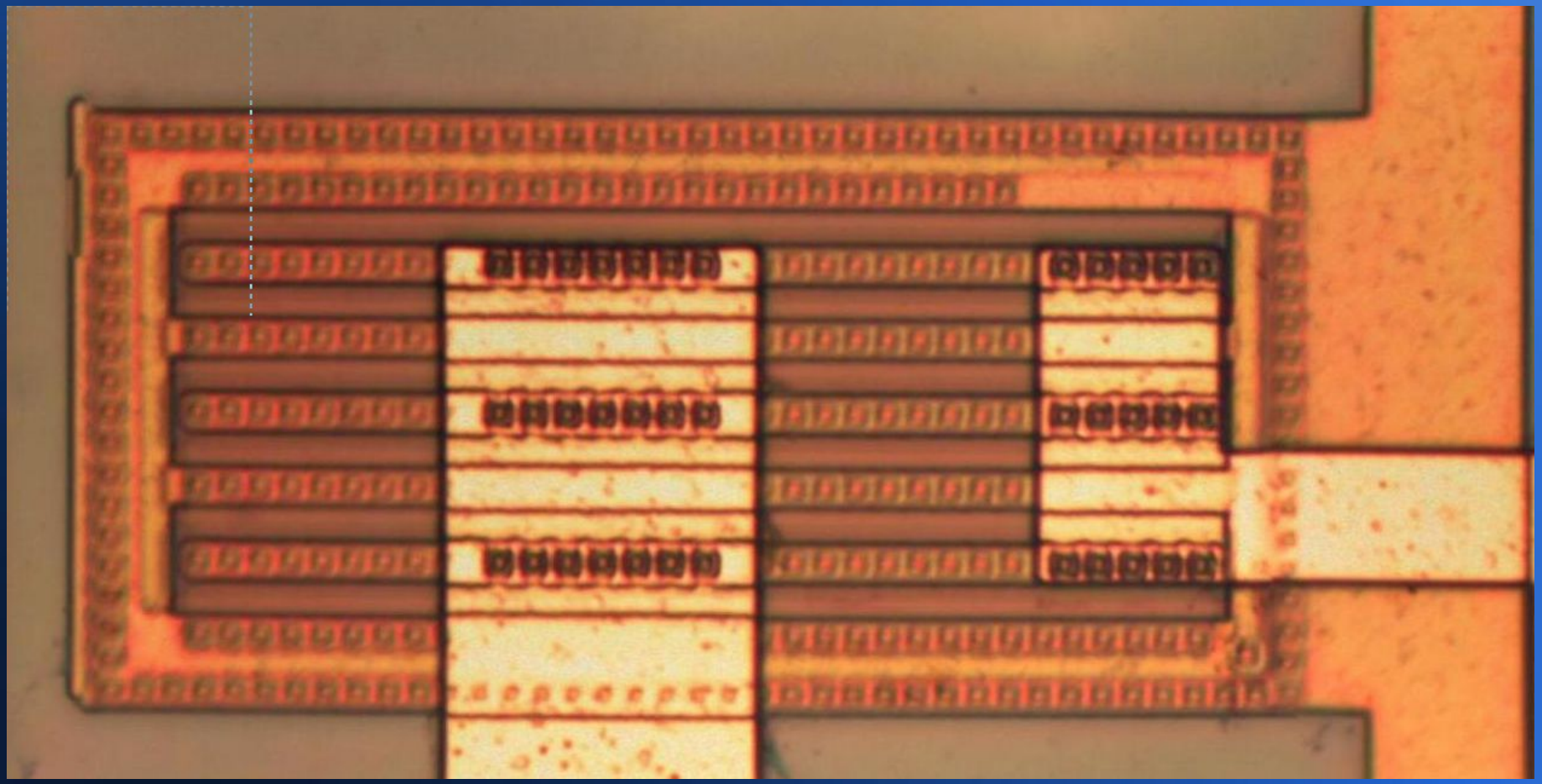
Small-signal diode



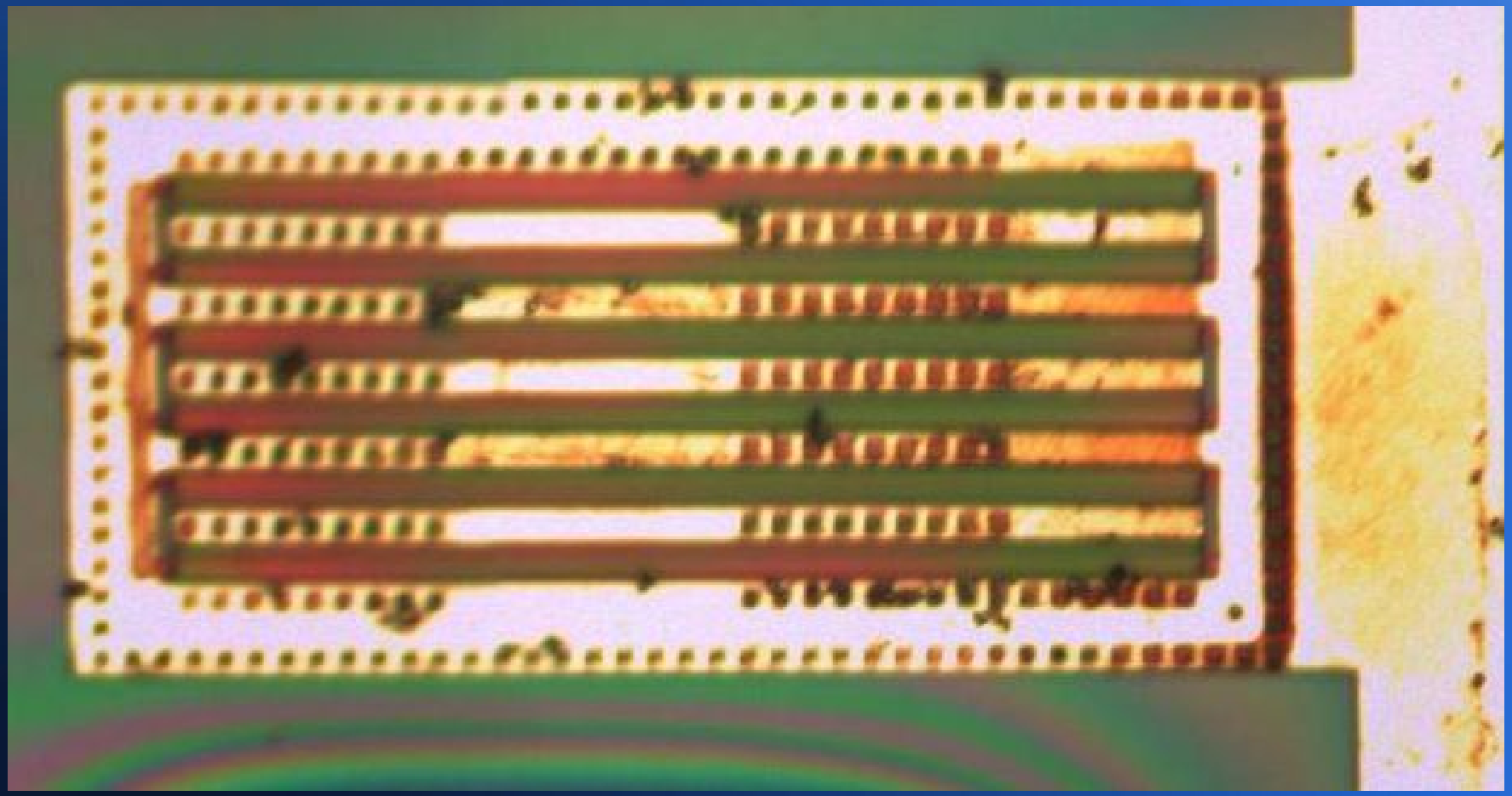
High-current diode



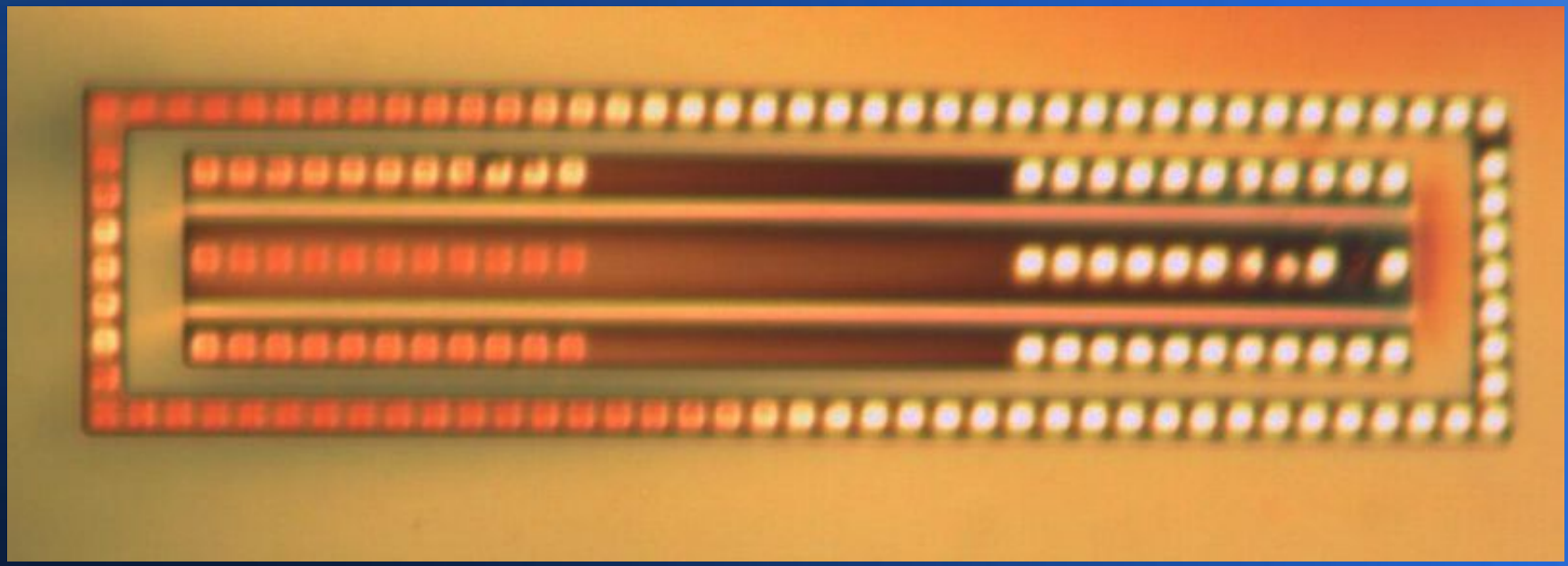
Actual diode (SecurID 600): M2



Actual diode: M1

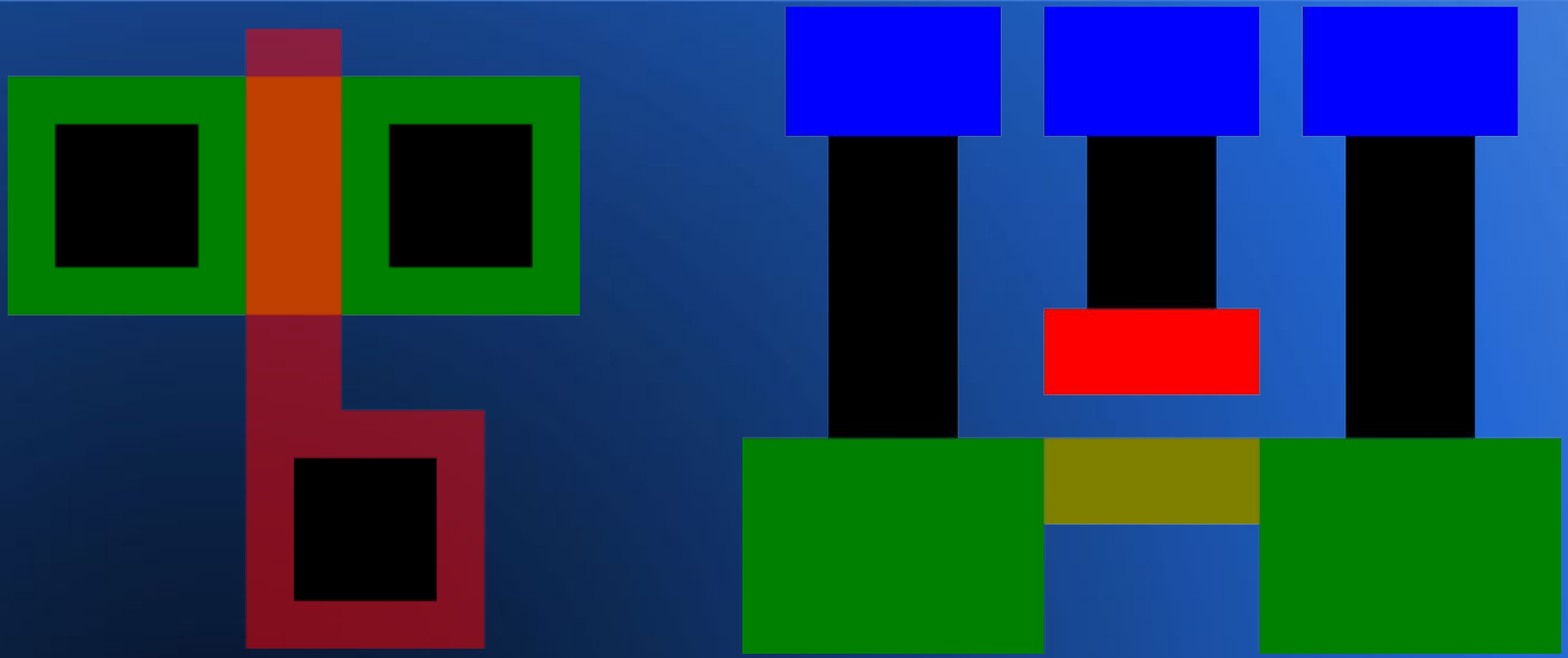


Actual diode: Implant

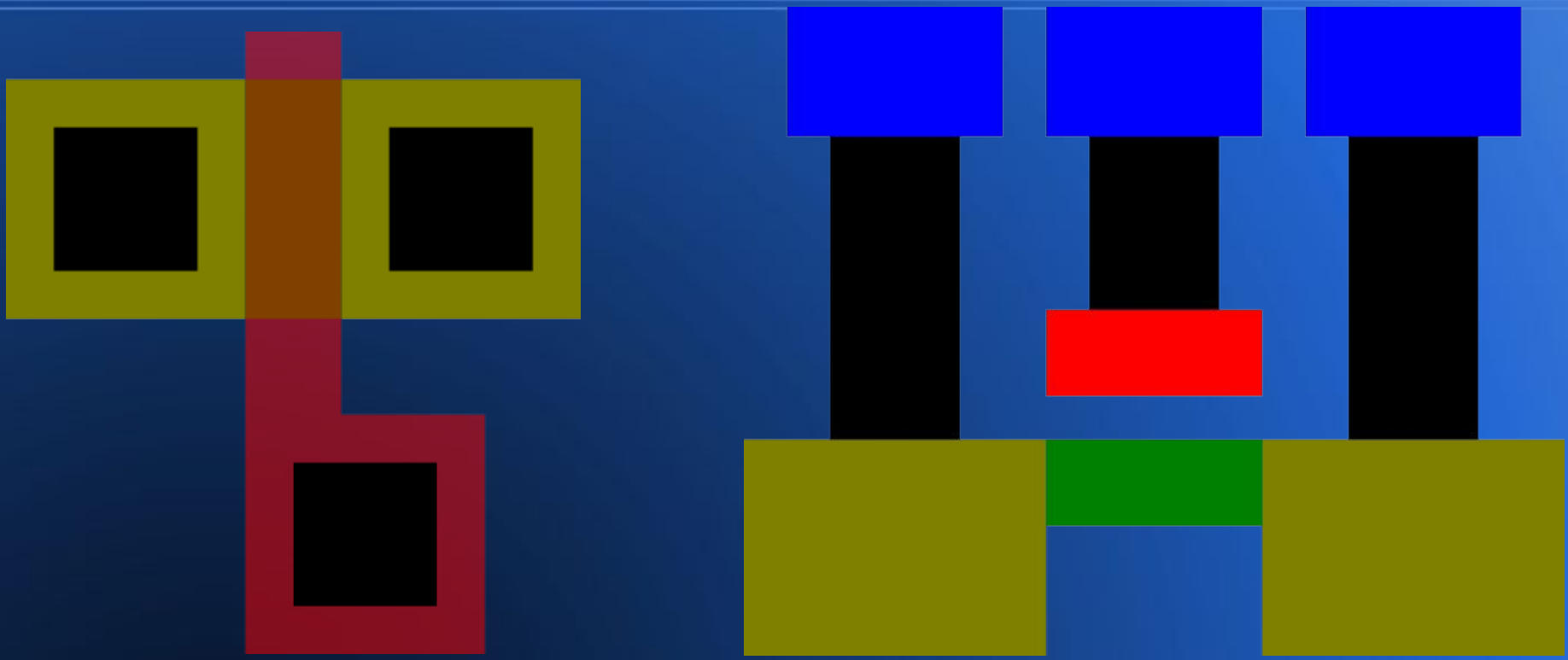


Not same diode as first two pics, that one was damaged during sample prep :(

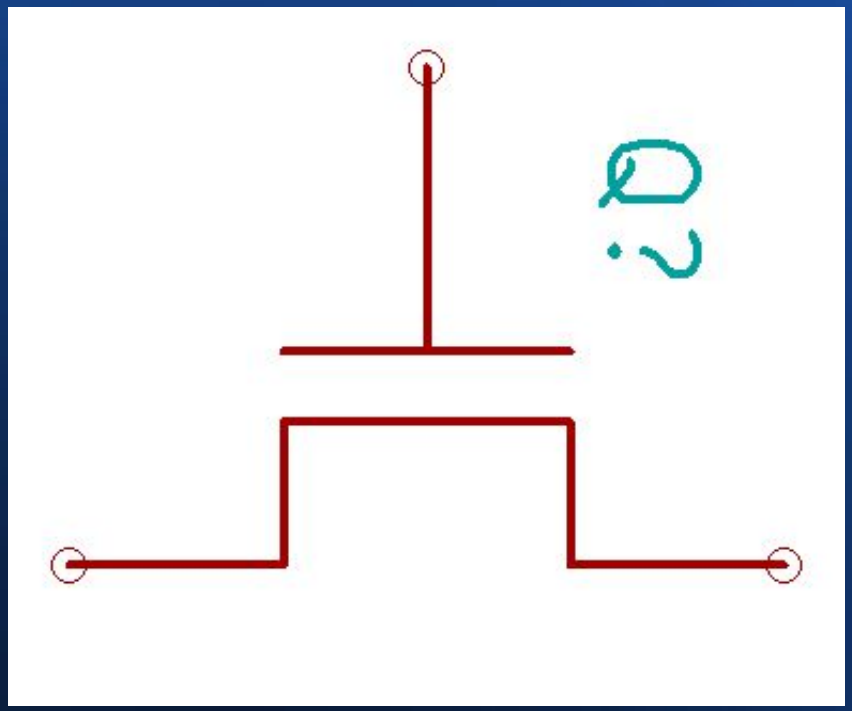
N-channel MOSFET

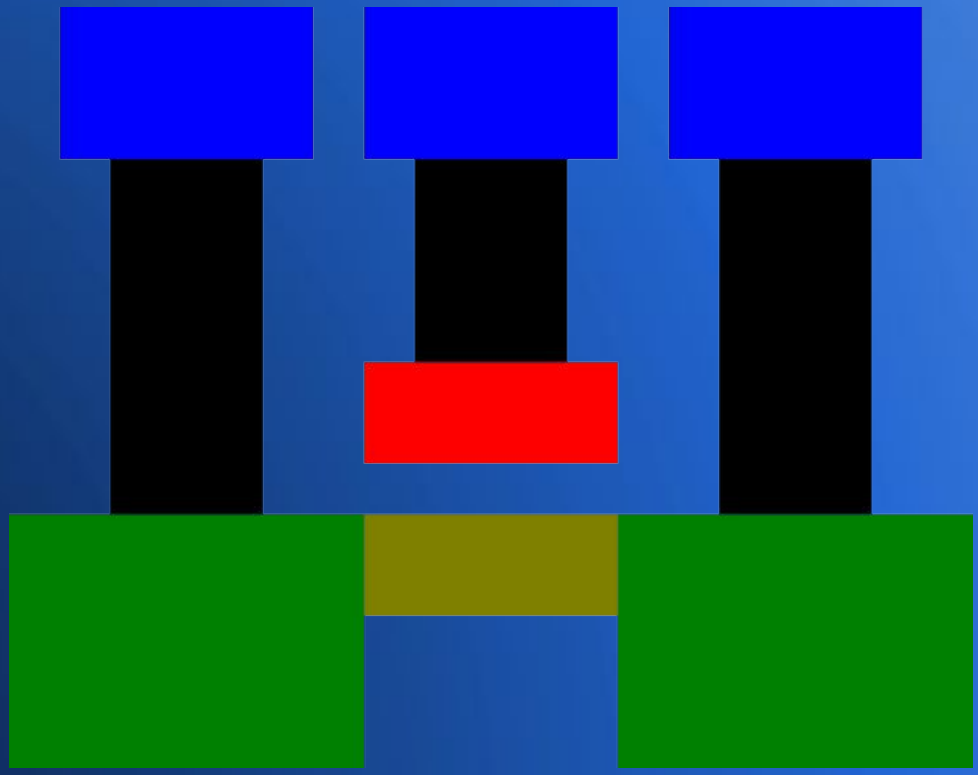


P-channel MOSFET

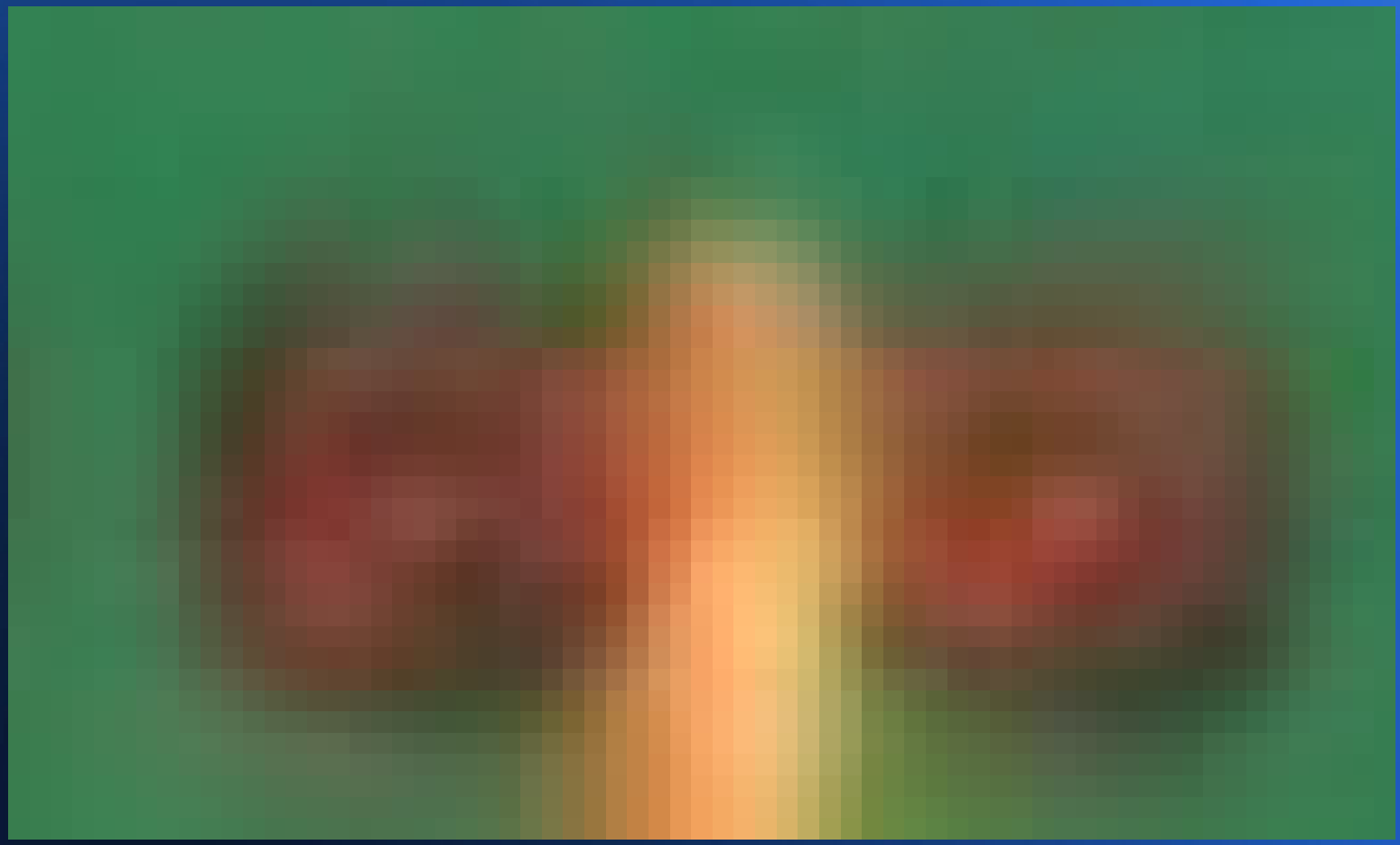


Schematic symbols

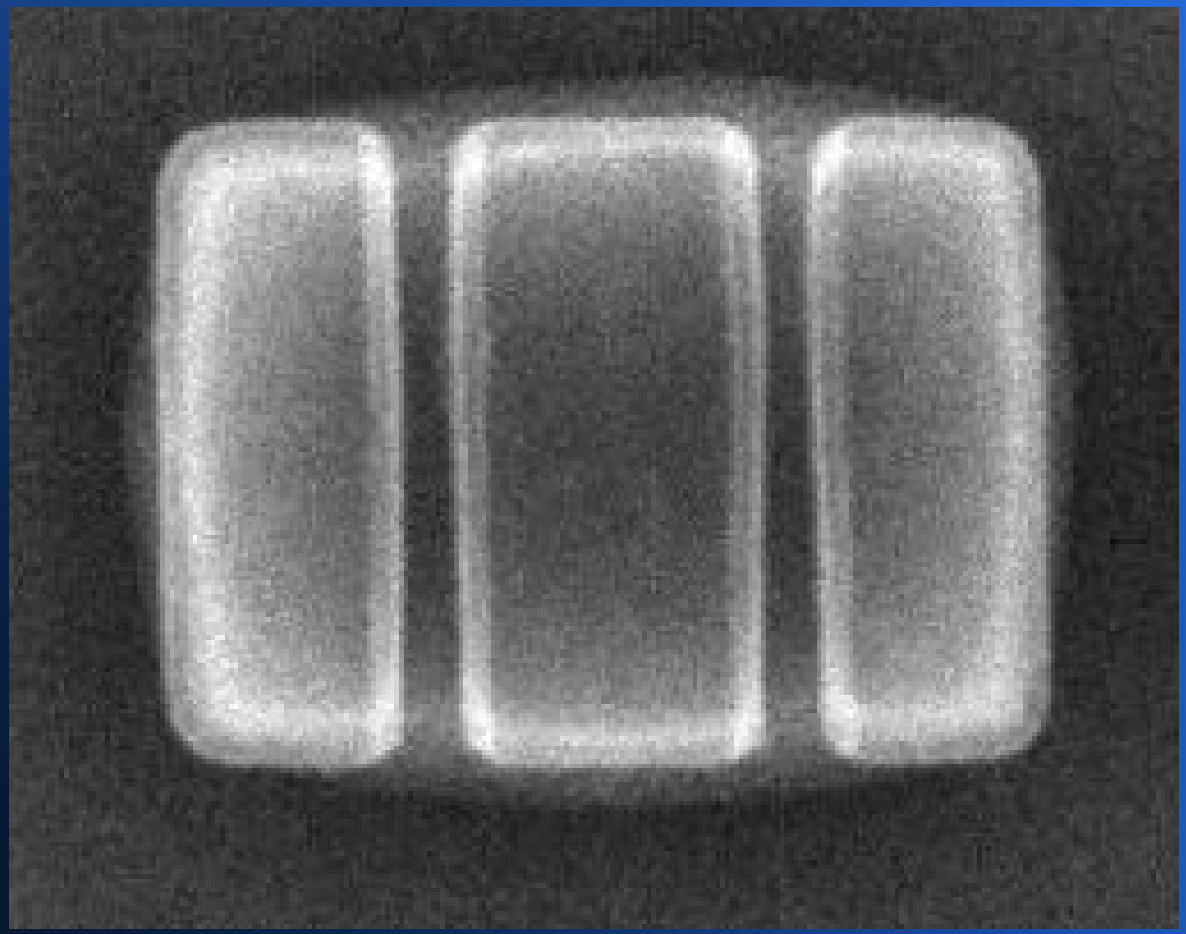




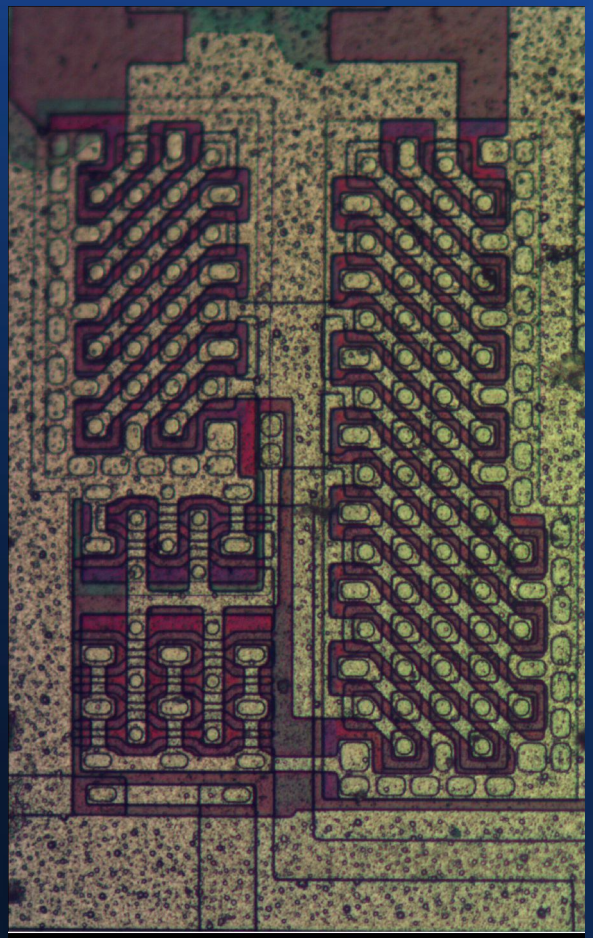
Actual small-signal NMOS

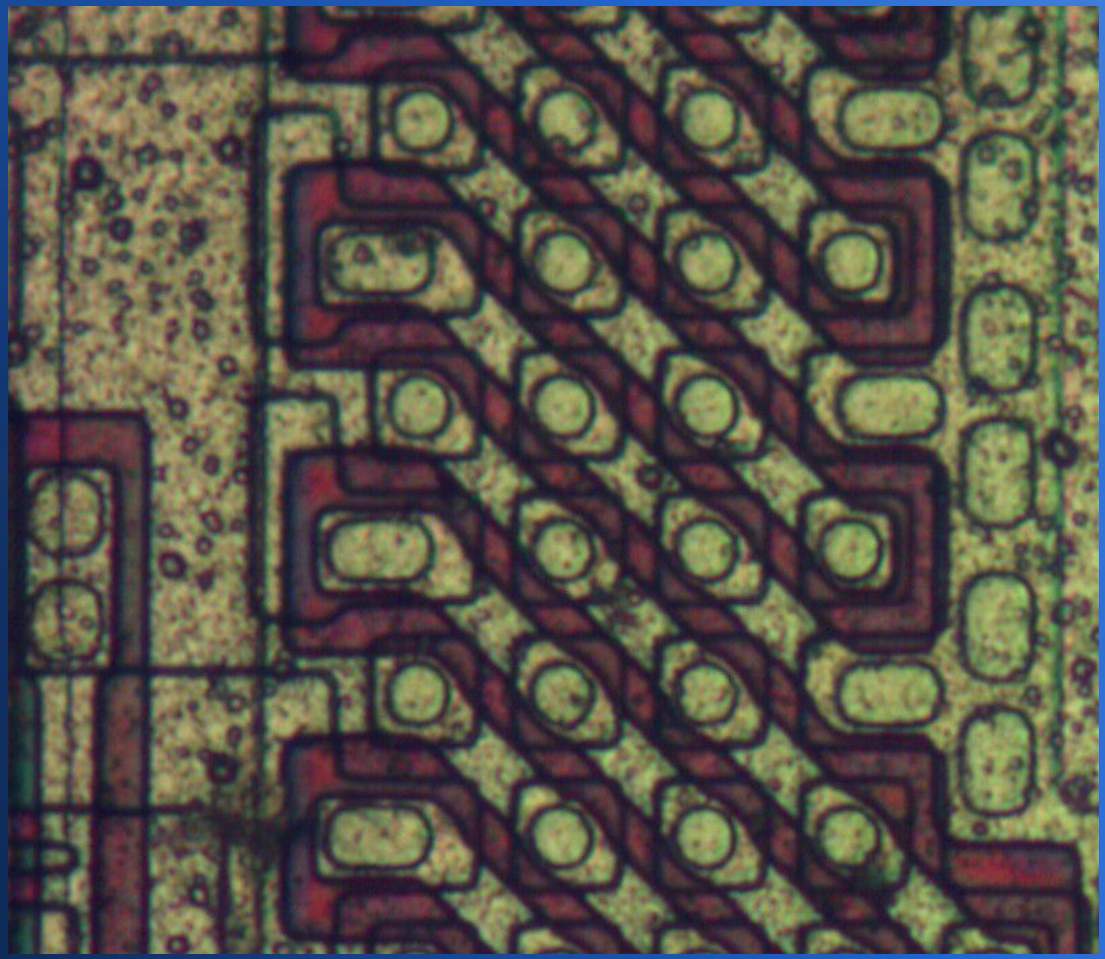


Dopant stain of two PMOS

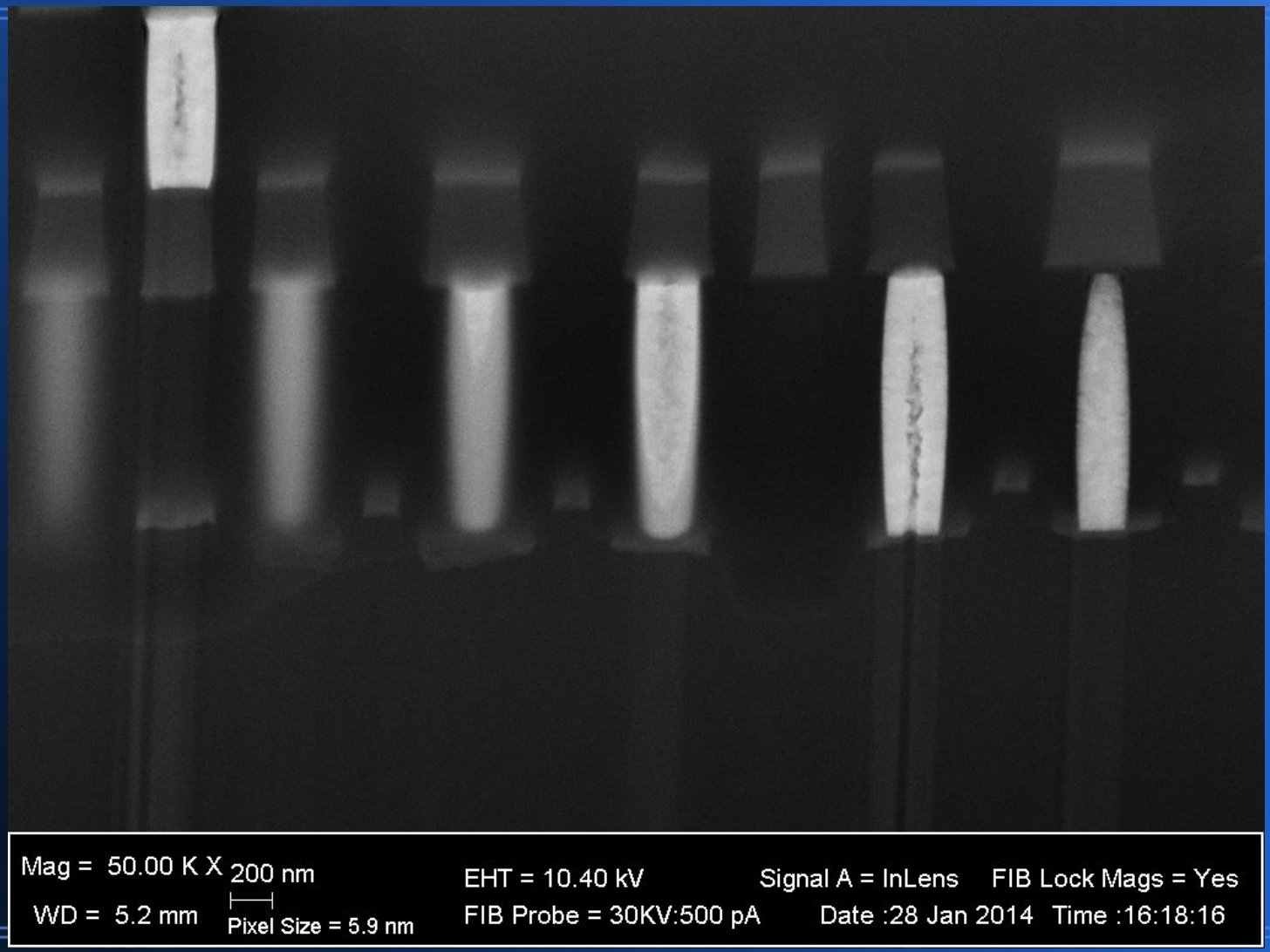


Actual pad-driver MOSFETs





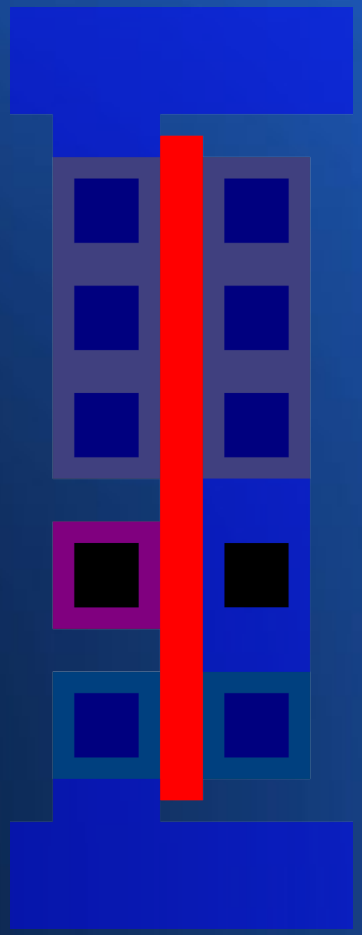
MOSFET cross section



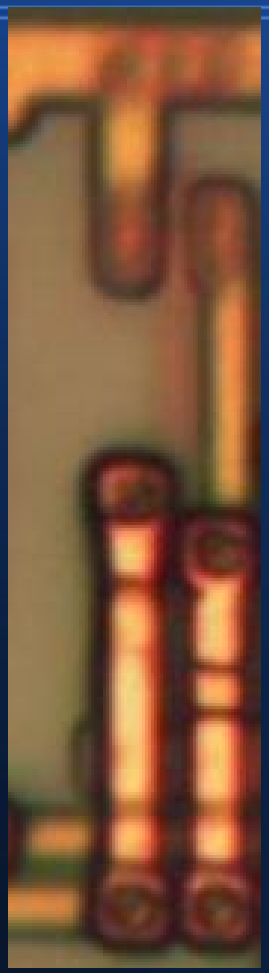
Transistor sizing

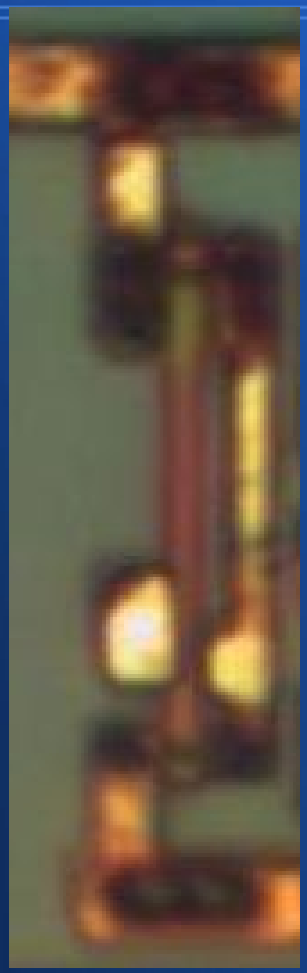
- Lots of tricks needed to get good performance
- Rds(on) of PMOS is ~2.5x NMOS
- Channel width increased to compensate

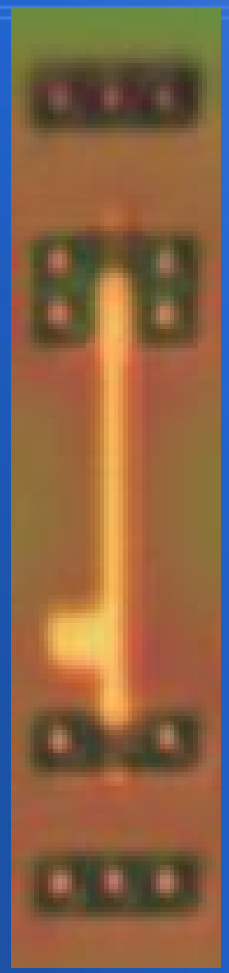
Putting it all together: Inverter



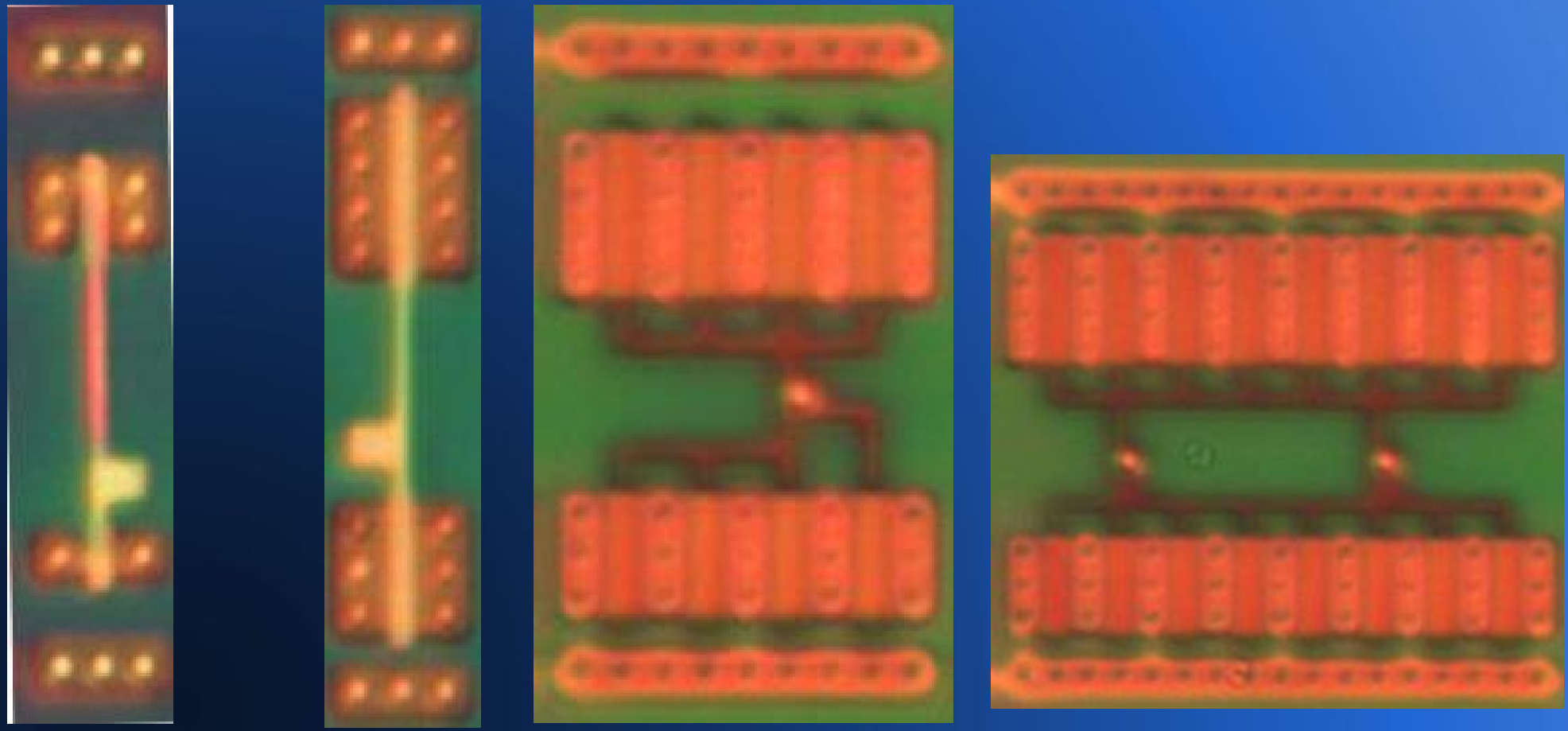
Actual inverter: SID600



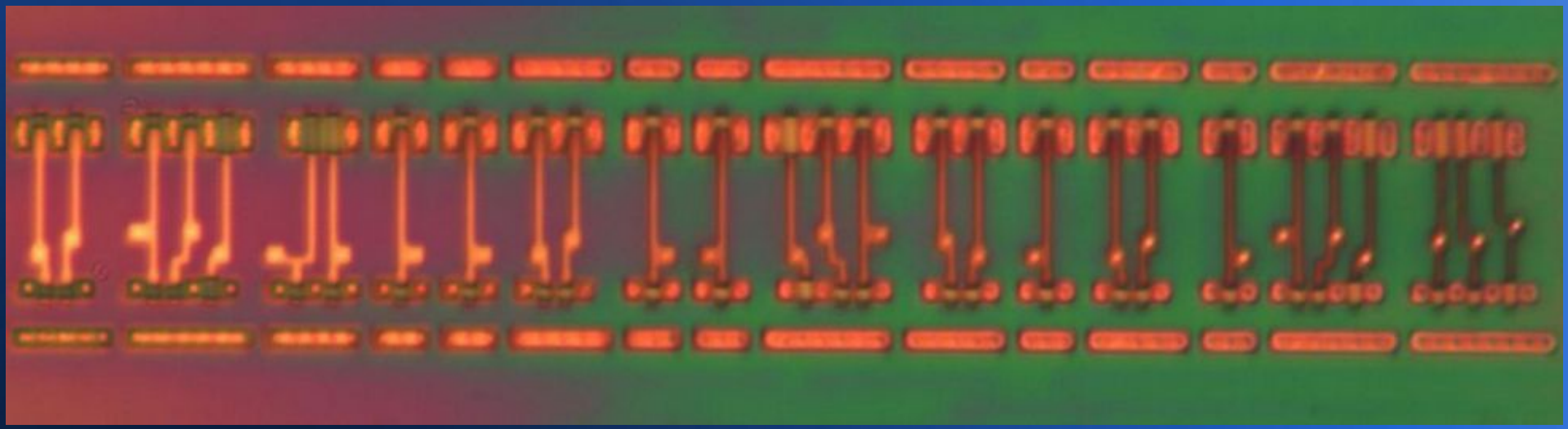




Varying drive strength

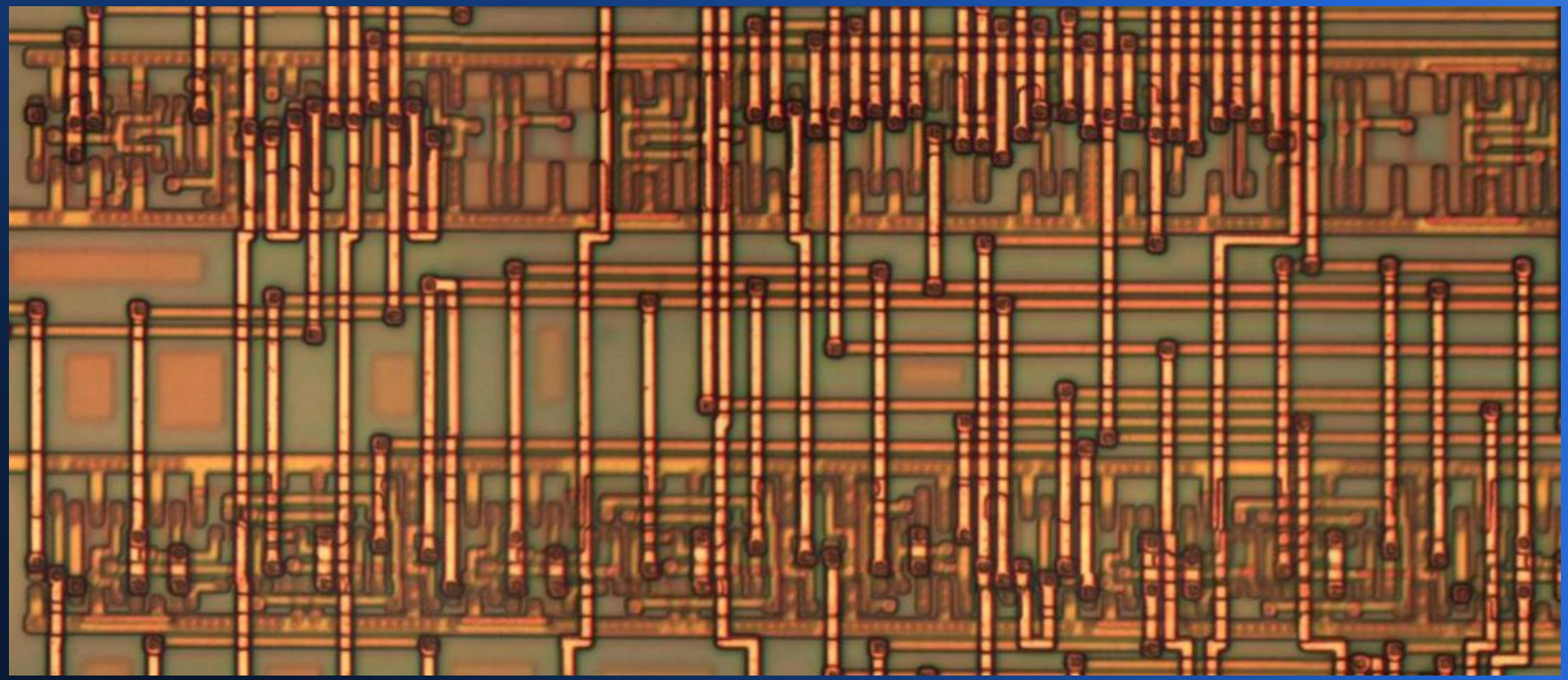


Standard cells



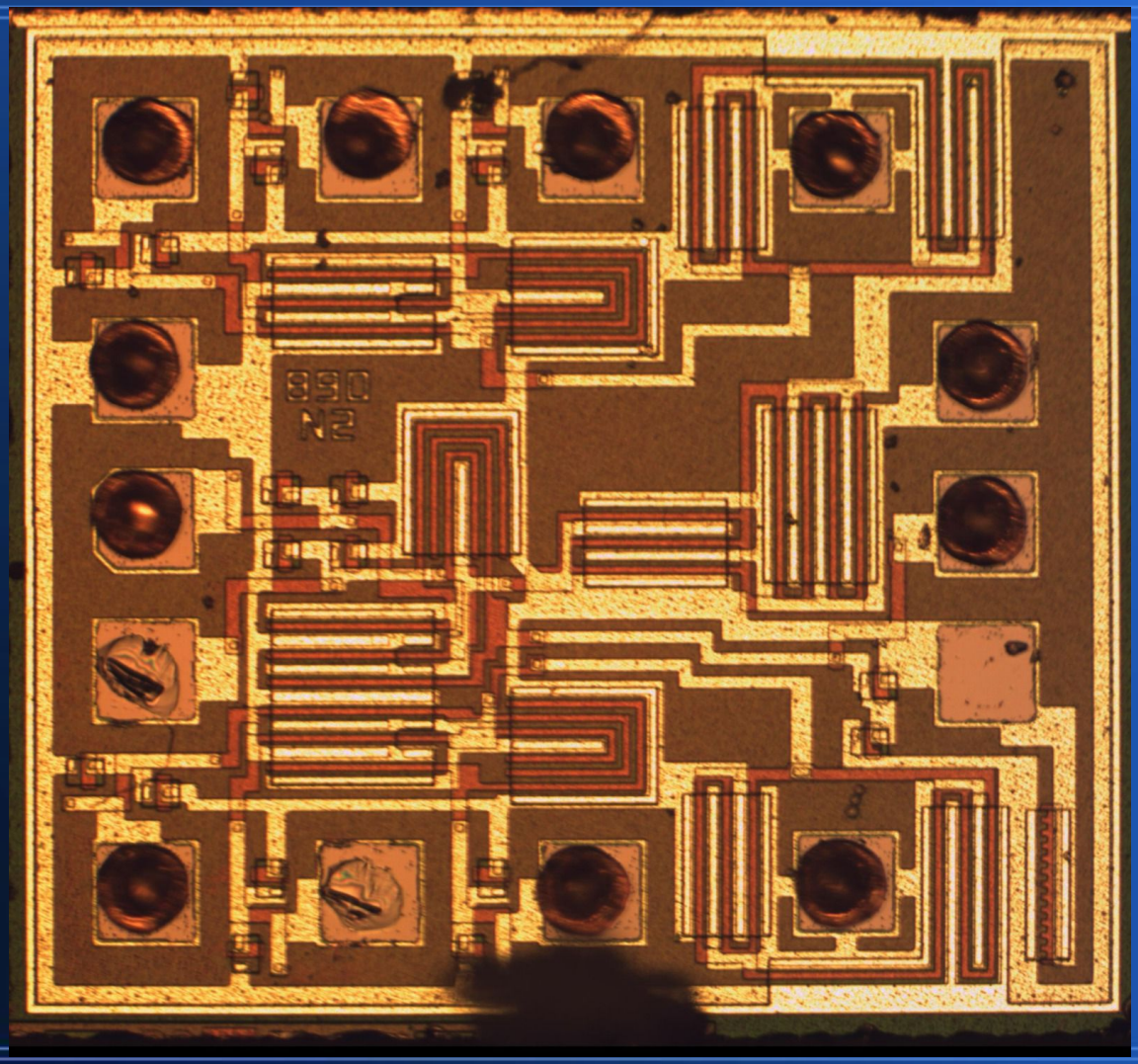
Standard cell routing

- Layers typically alternate X and Y axes

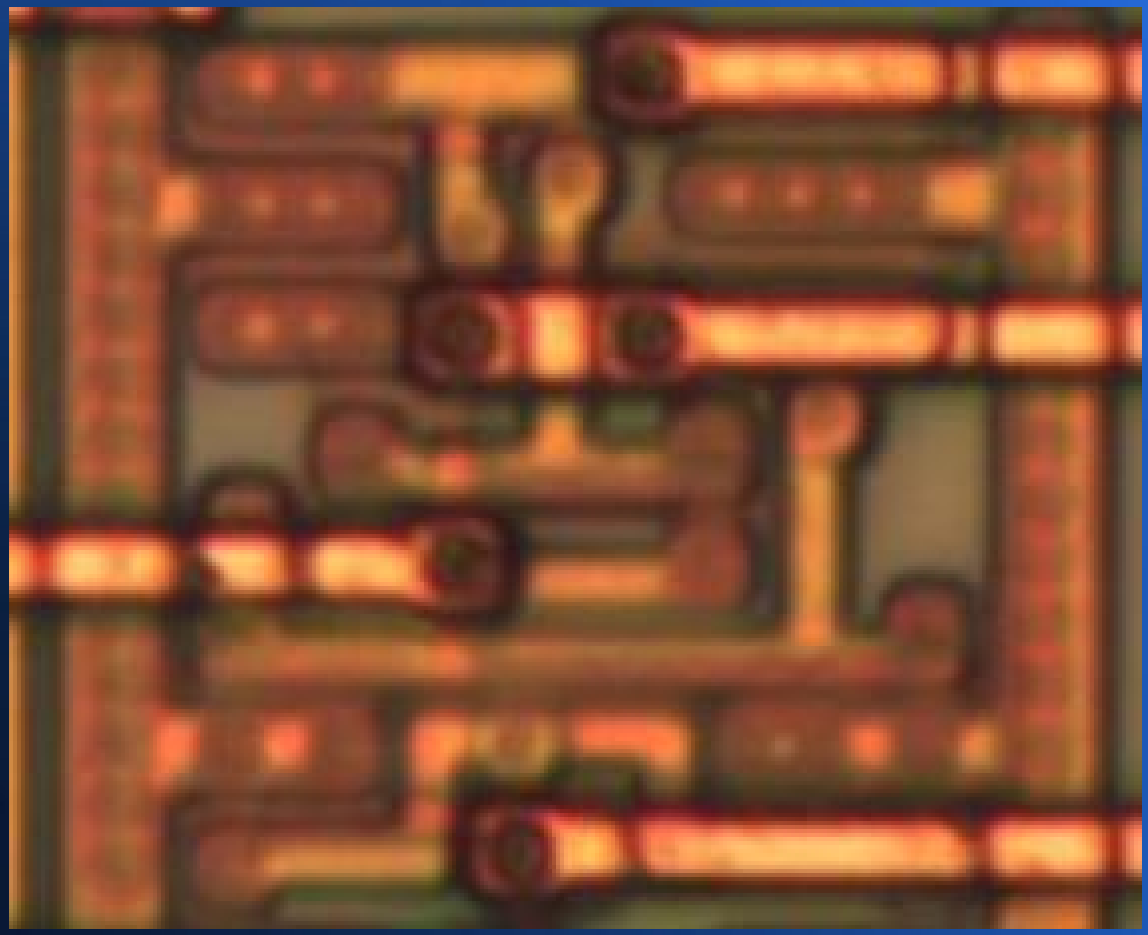


- Demo of vectorization

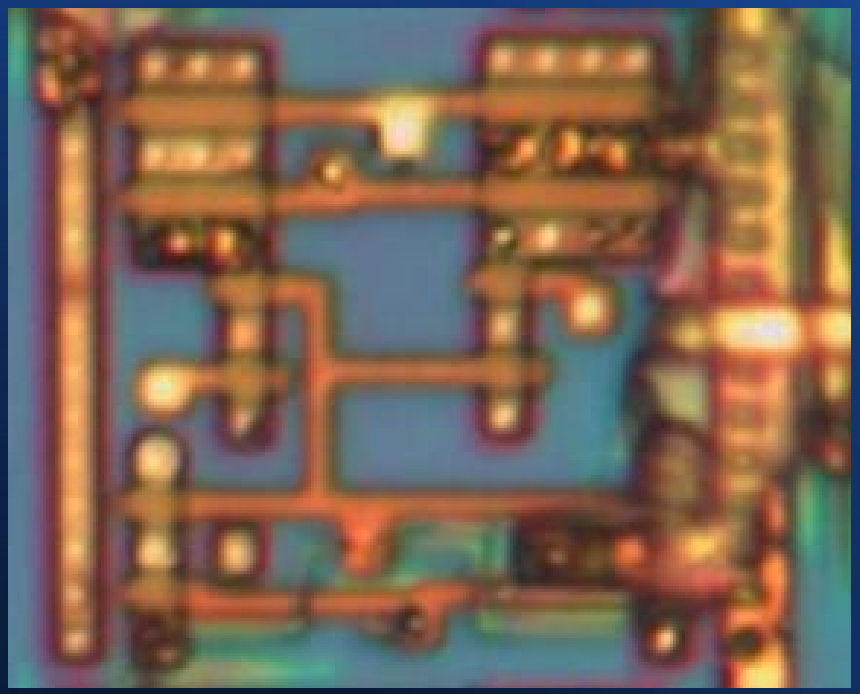
In-class exercise 1

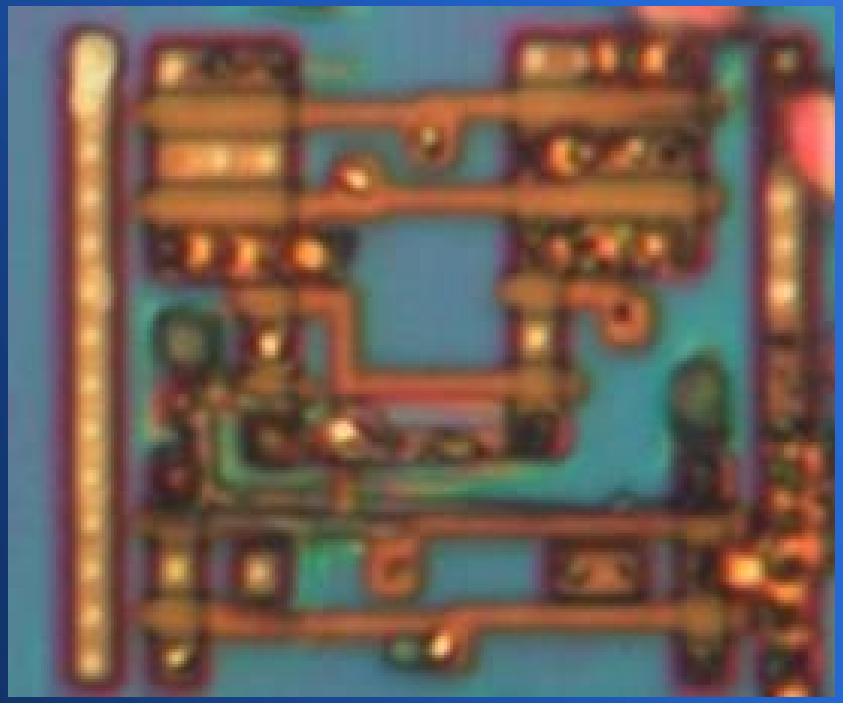


In-class exercise 2: Metal



In class exercise 2: Poly





In class exercise 2: Active

Questions?

- TA: Andrew Zonenberg <azonenberg@drawersteak.com>
- Image credit: Some images CC-BY from:
  - John McMaster <JohnDMcMaster@gmail.com>