CSCI 4974 / 6974
Hardware Reverse Engineering

Lecture 11: RAM

Types of RAM

- Static RAM (SRAM)
- Dynamic RAM (DRAM)
- Other esoteric types

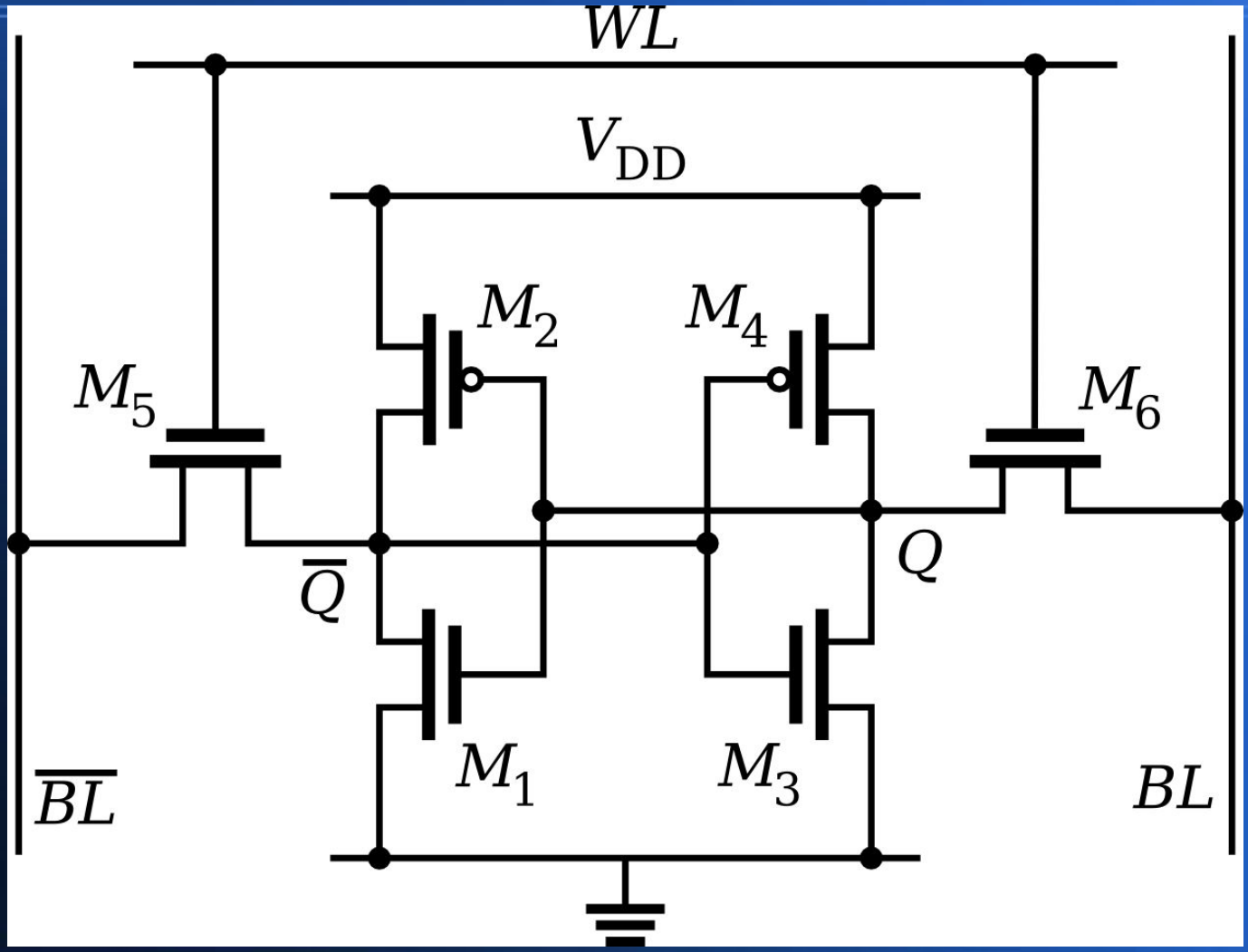
SRAM

- Static RAM
- Basic cell is essentially a D latch
- Less dense (6-8 transistors per cell)
- Commonly used for MCU main memory, small buffers, CPU caches, etc
- Holds data indefinitely as long as power is applied

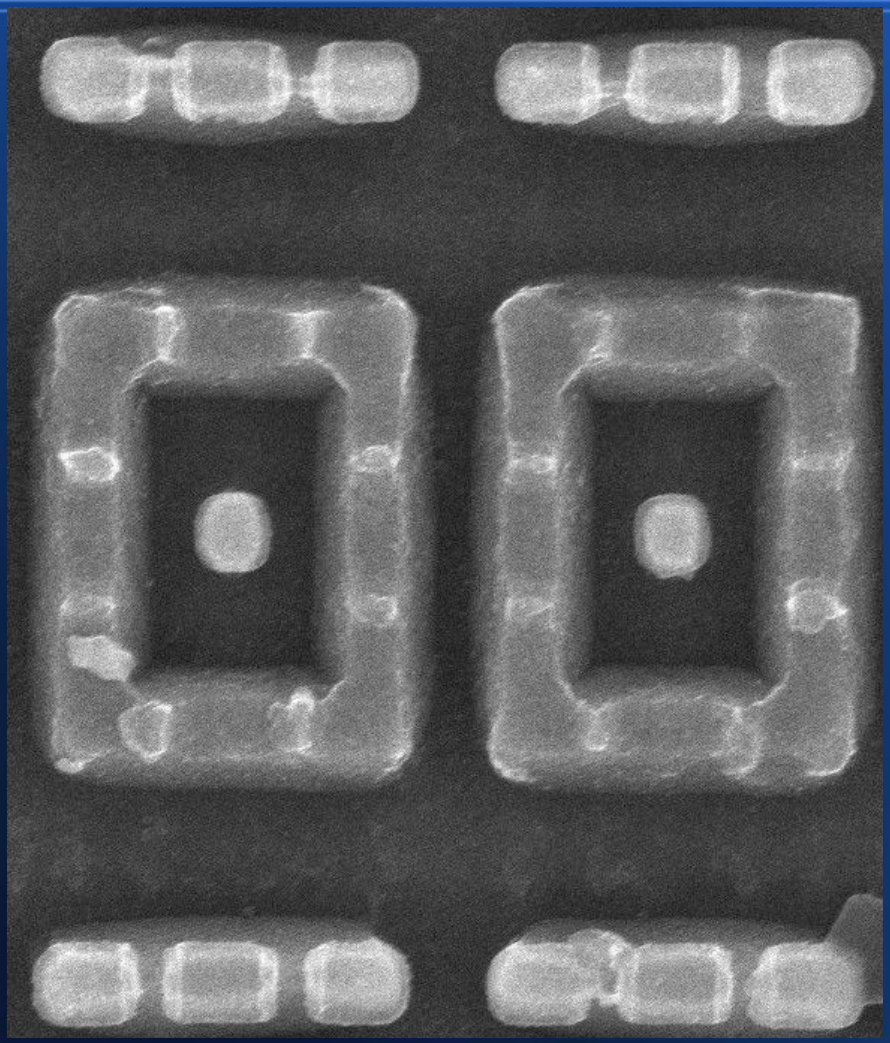
6T SRAM

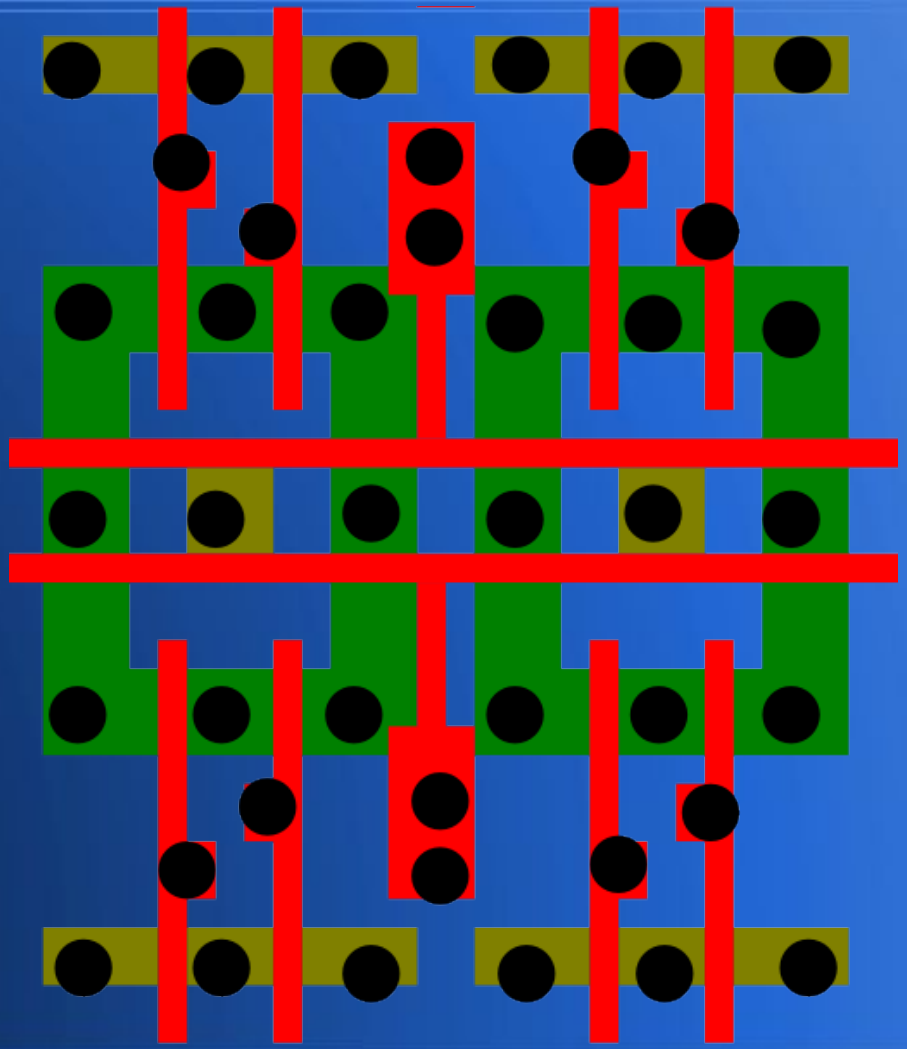
- 4 NMOS, 2 PMOS per unit cell
- Normally organized in 2D grid
- Differential bit lines + pwr run on metal
  - Single ended r/w is possible in theory, but much less robust so rarely used
- Perpendicular word lines on poly (+ metal)

6T SRAM schematic

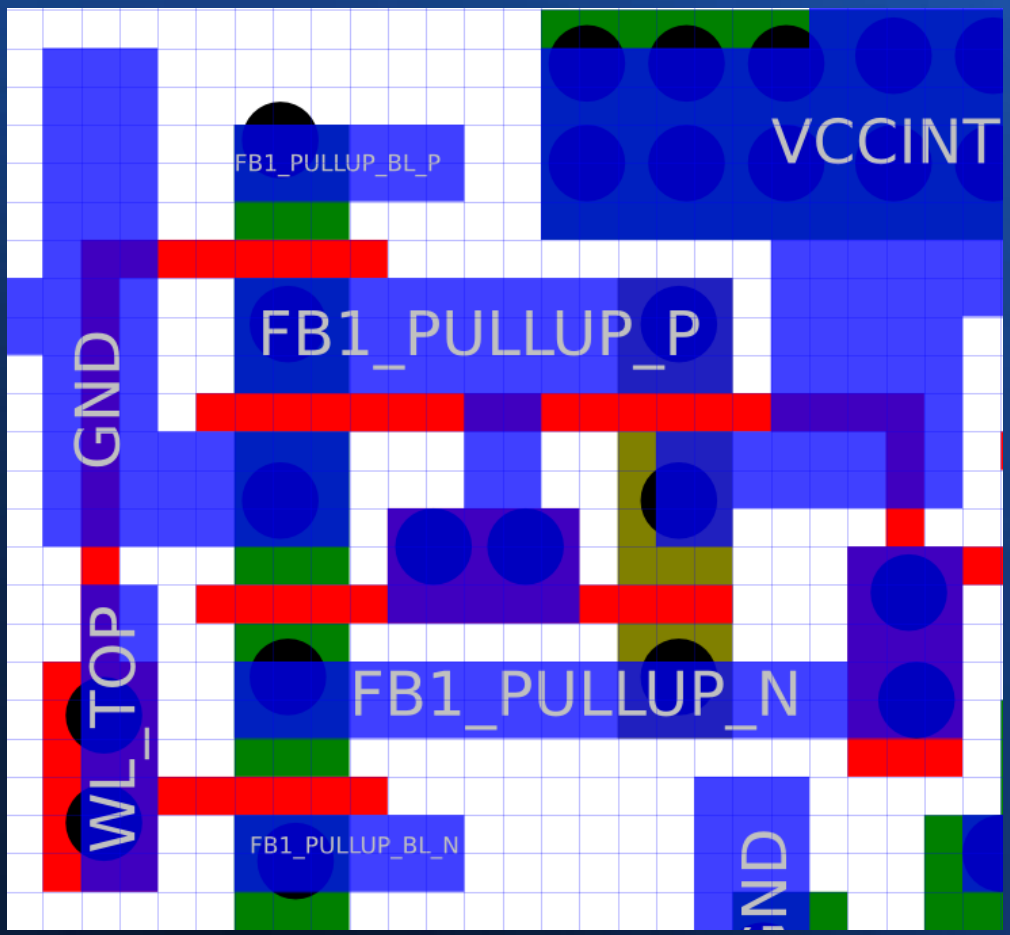


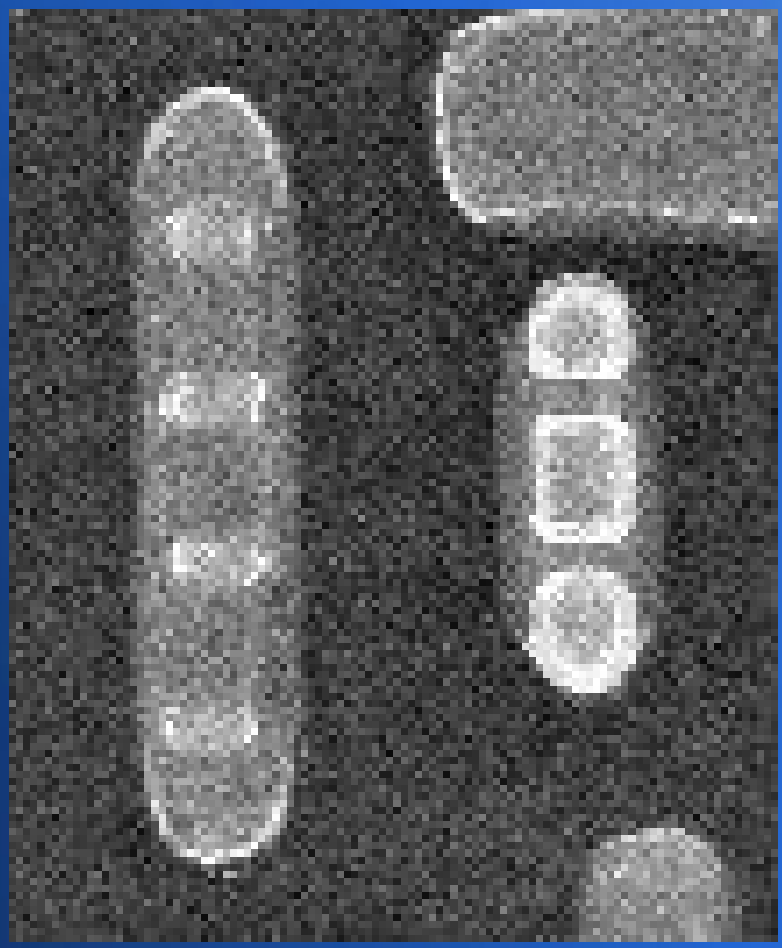
XC2C32A SRAMv1x1 (6T)



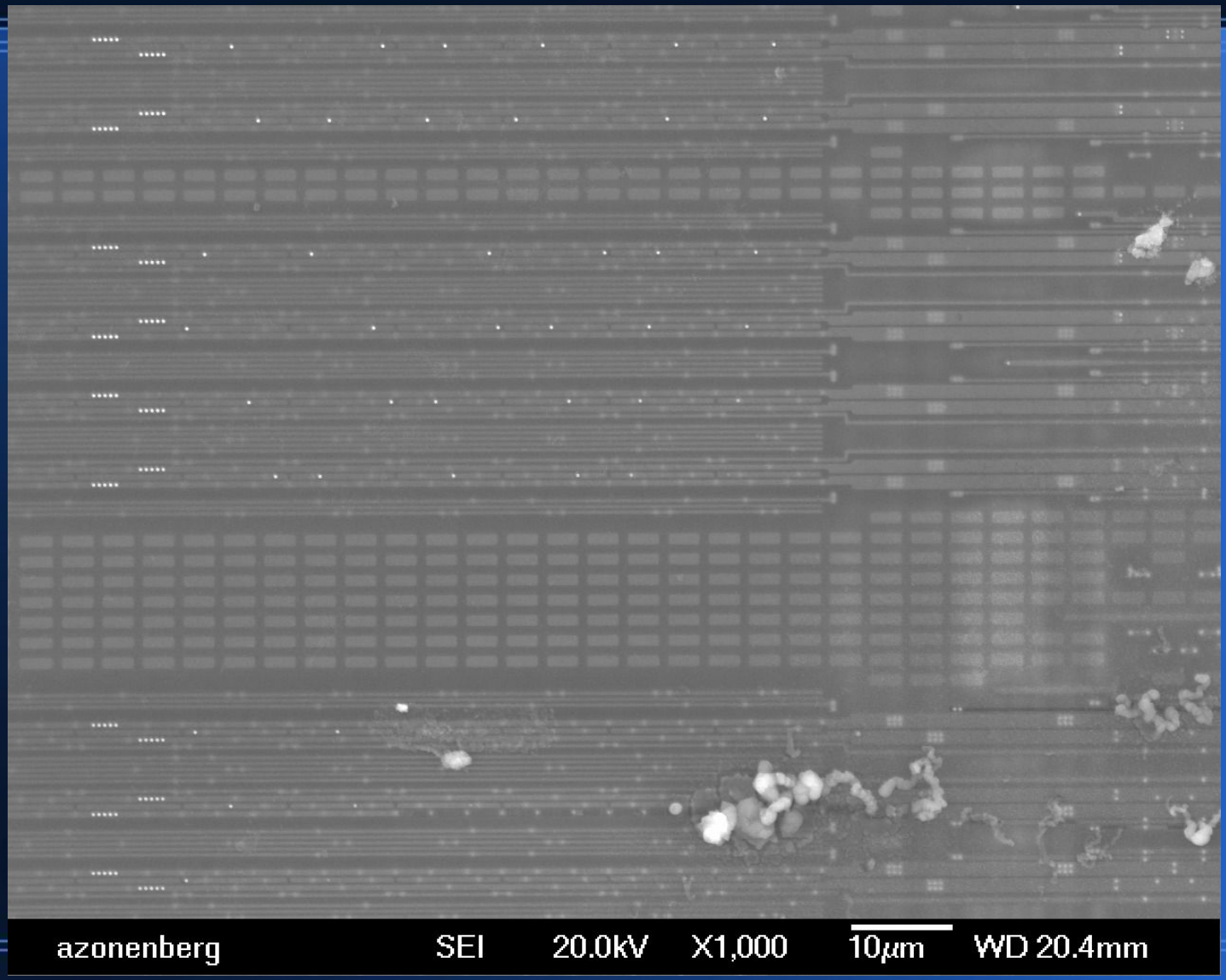


XC2C32A SRAMv0x1 (6T)

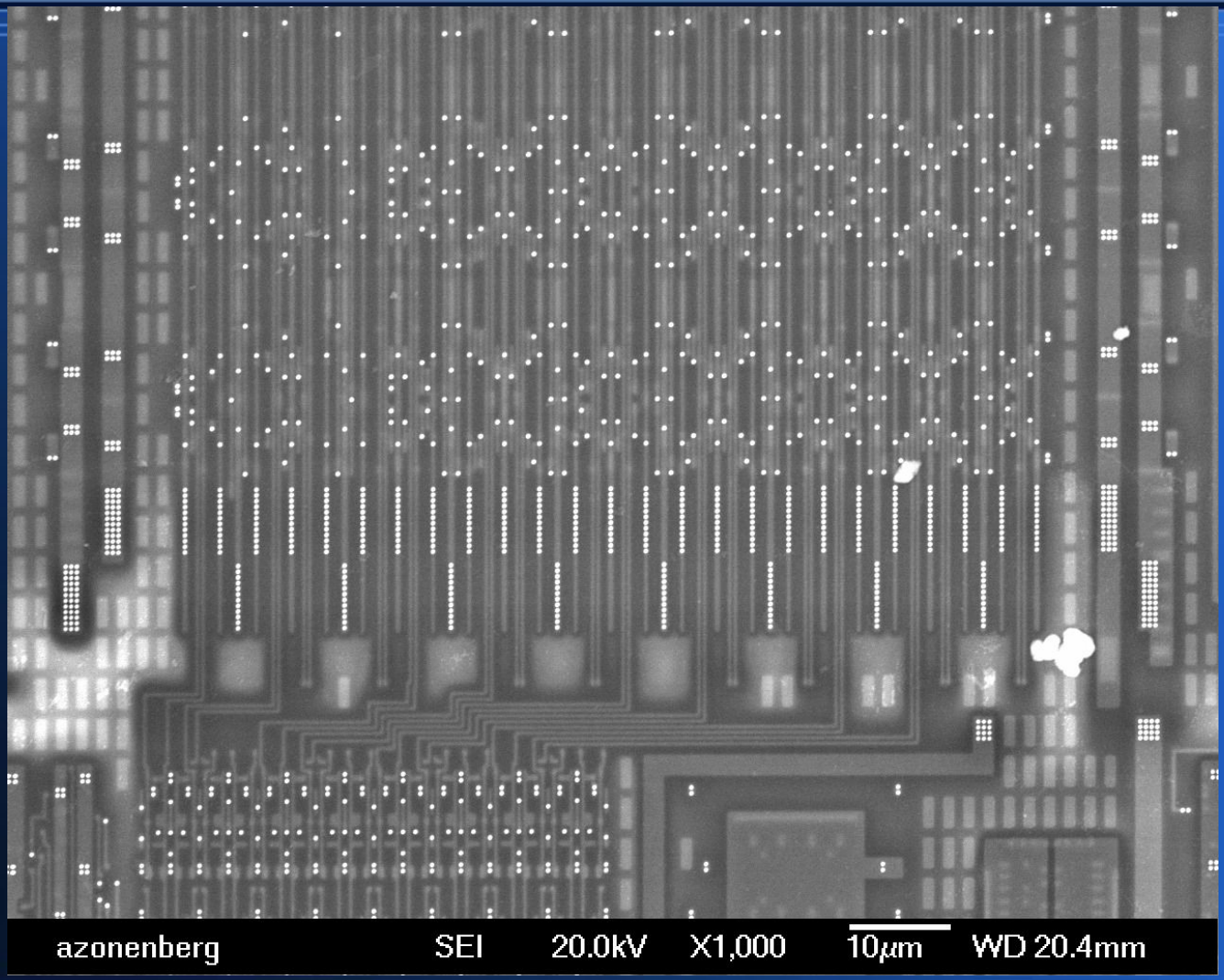




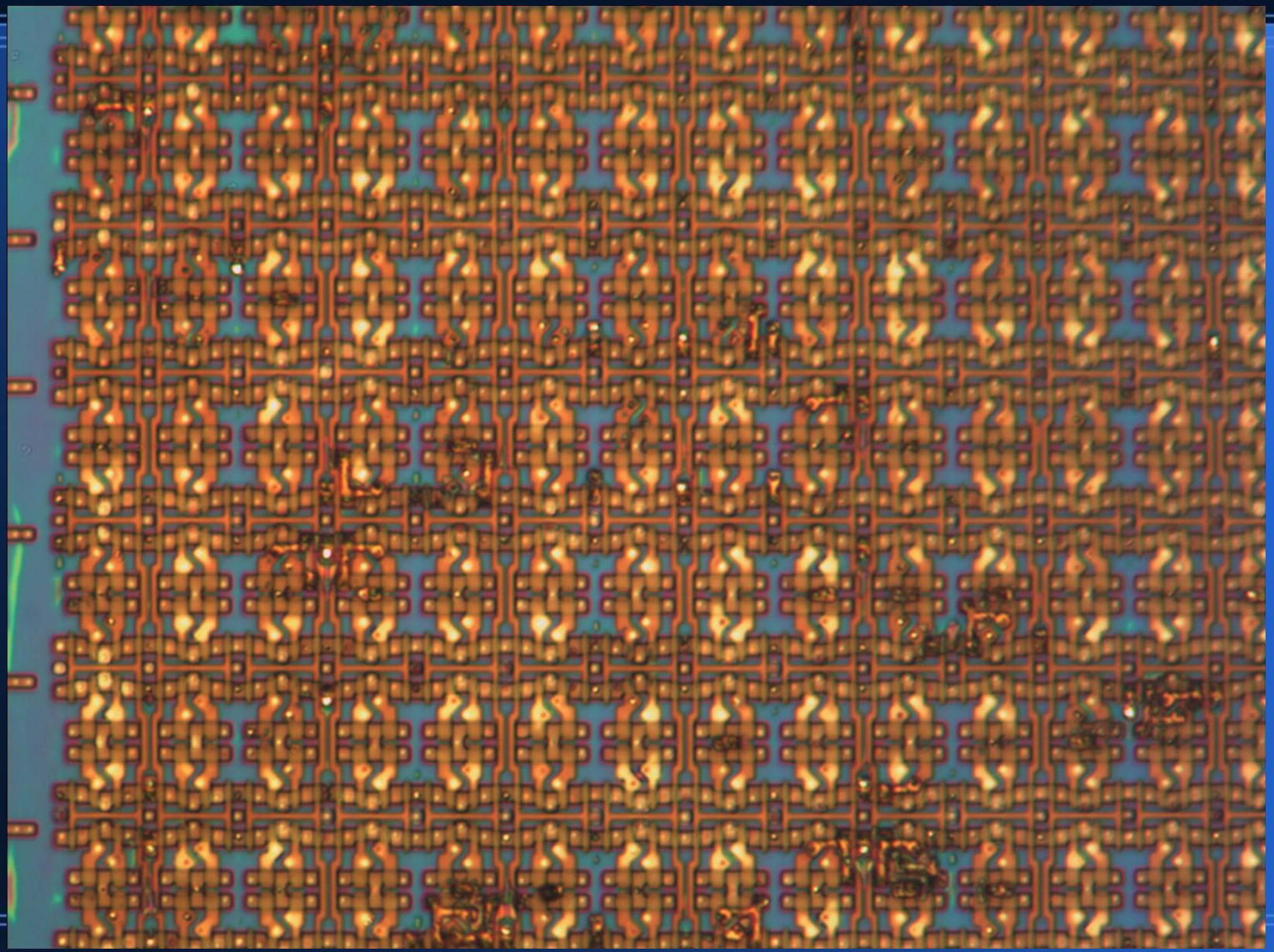
XC2C32A SRAM WLs



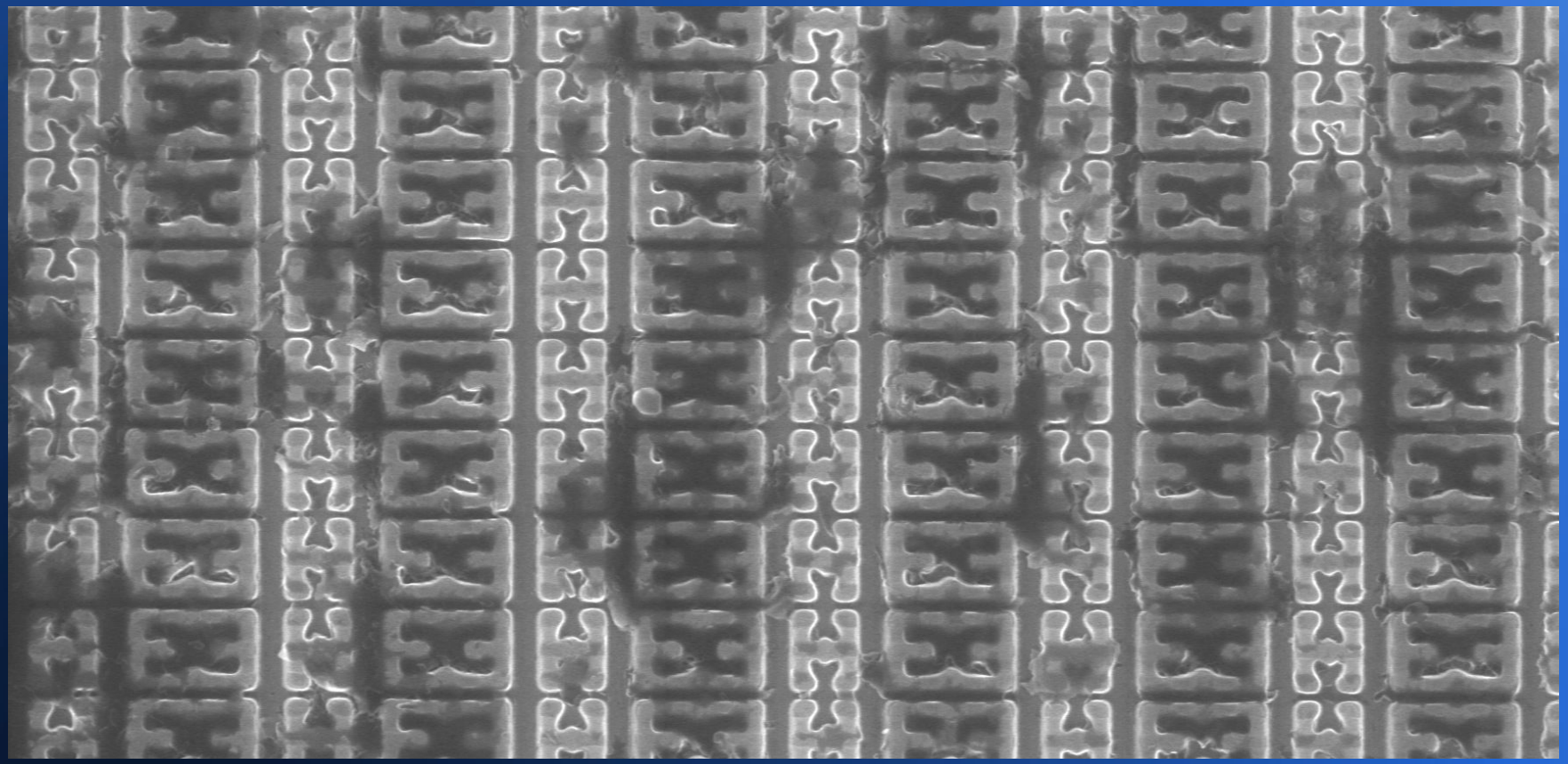
XC2C32A SRAM BLs



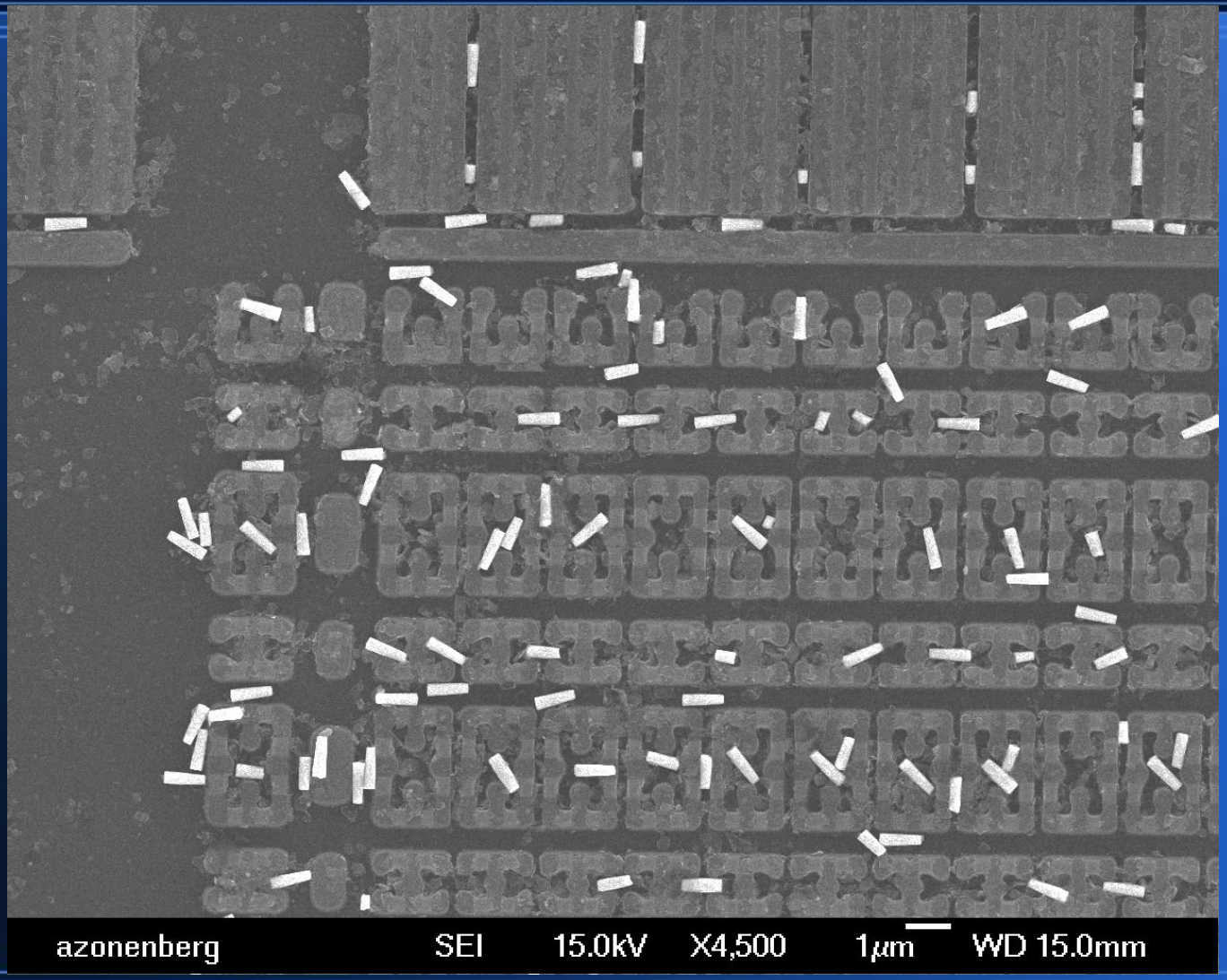
RSA SecurID SRAM (6T)



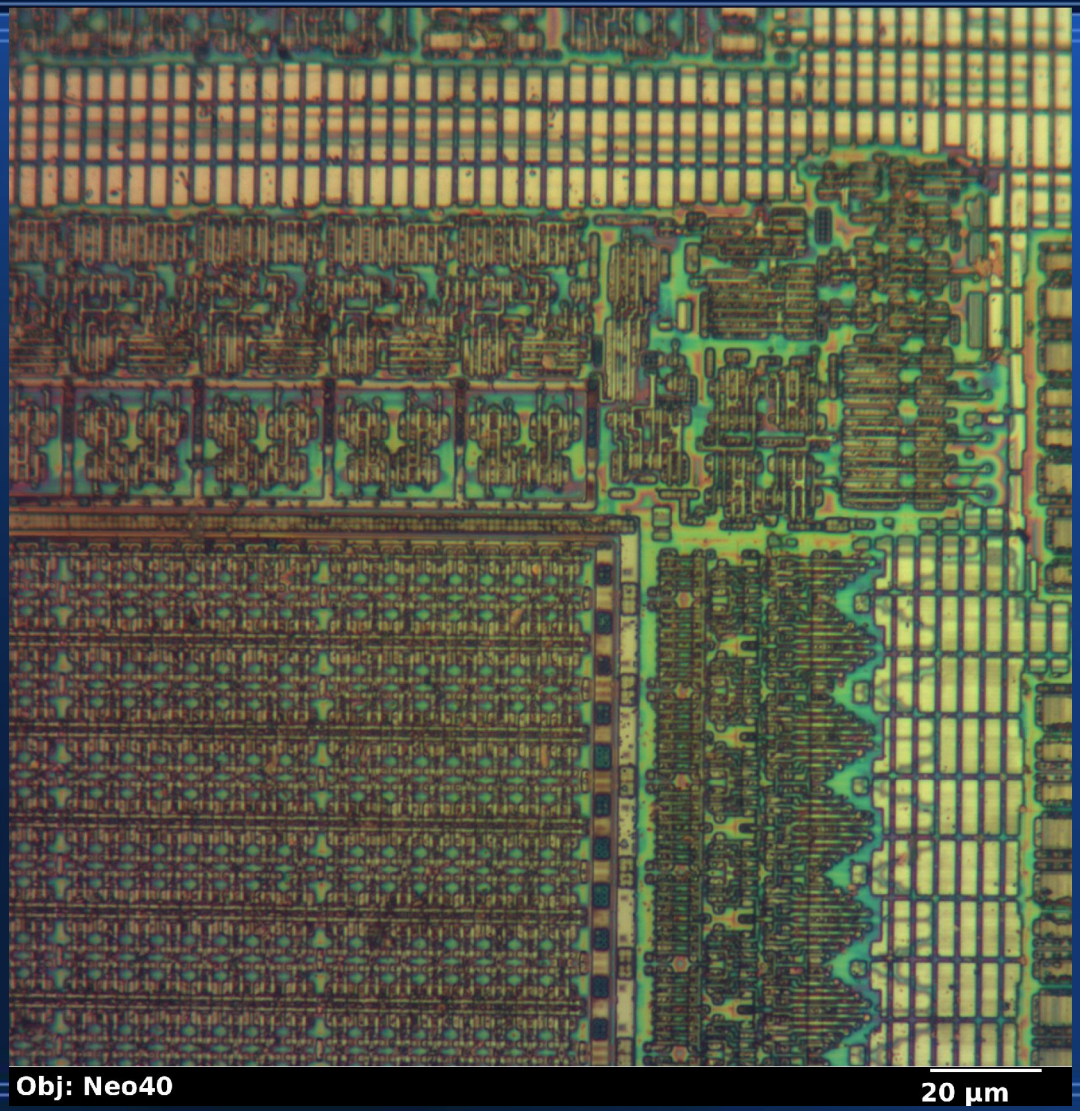
STM32 SRAM (6T)

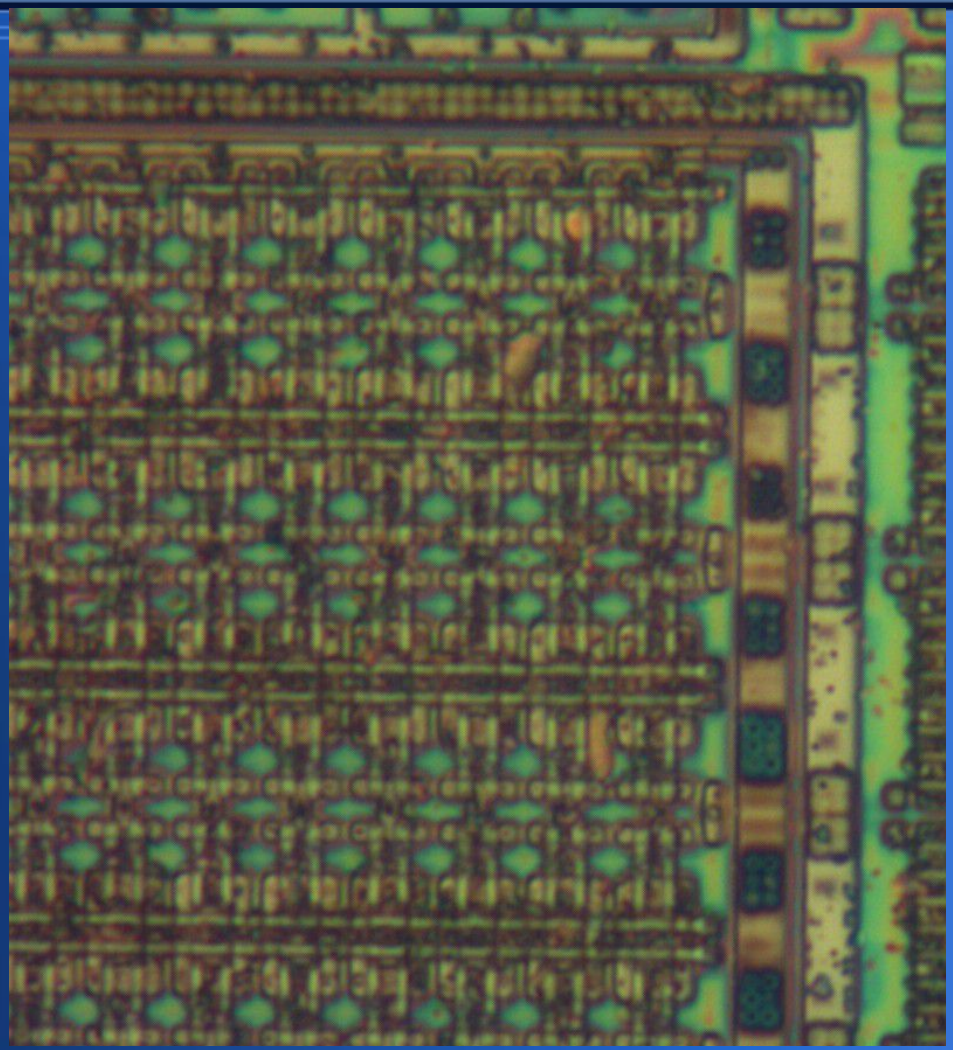


PIC32MX340F512H SRAM (6T)



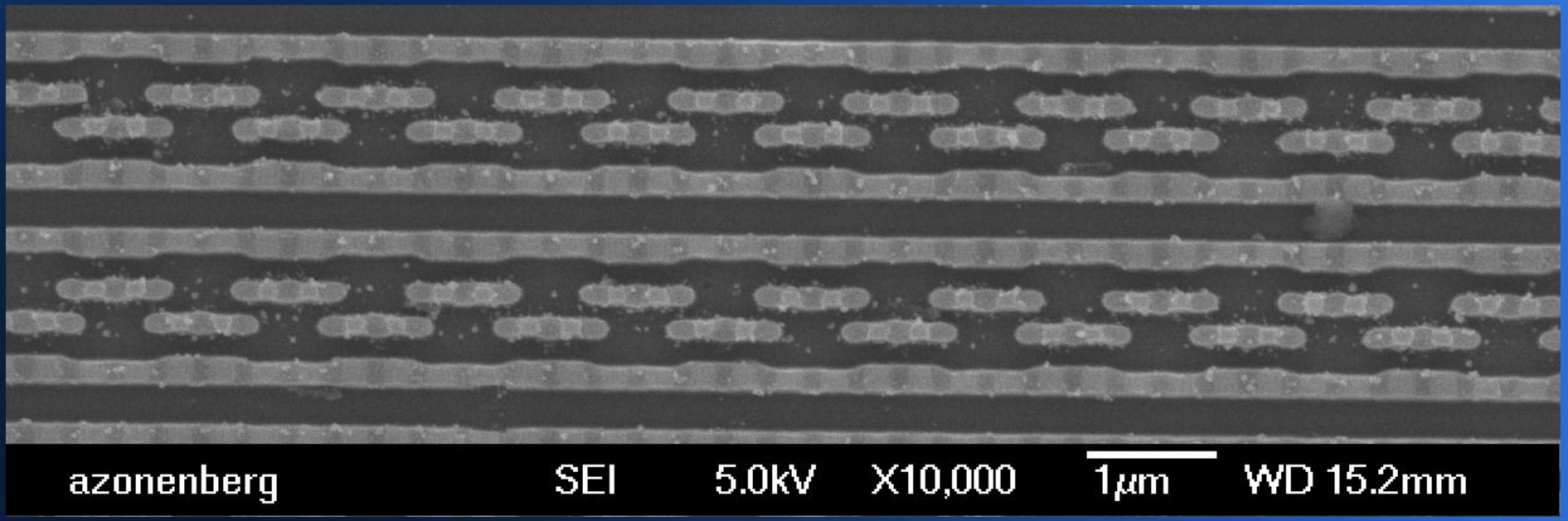
PIC12F683 SRAM (6T)





Lithography-optimized 6T cell

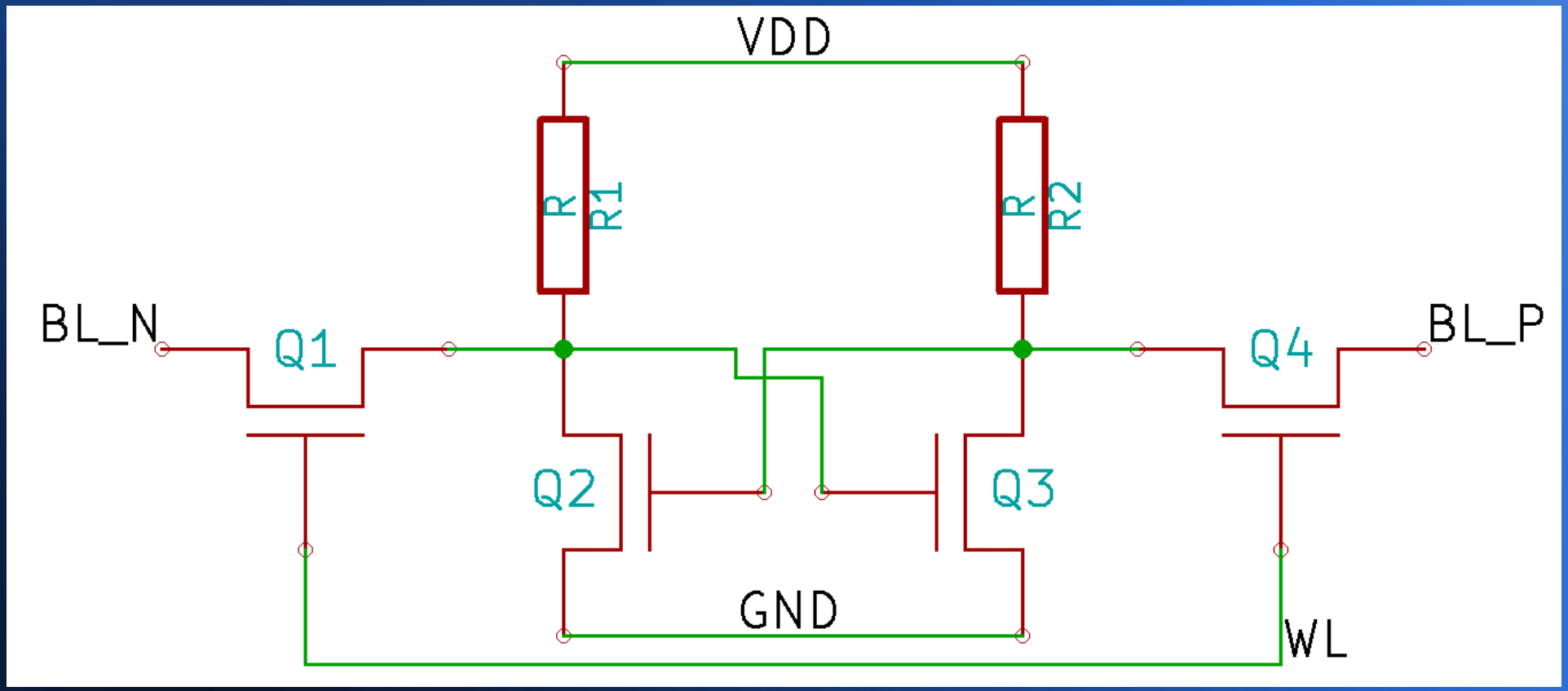
- Re-layout of textbook 6T cell
  - Parallel lines are easy to manufacture
- Example from PIC32MZ2048ECH (130 nm)



4T SRAM

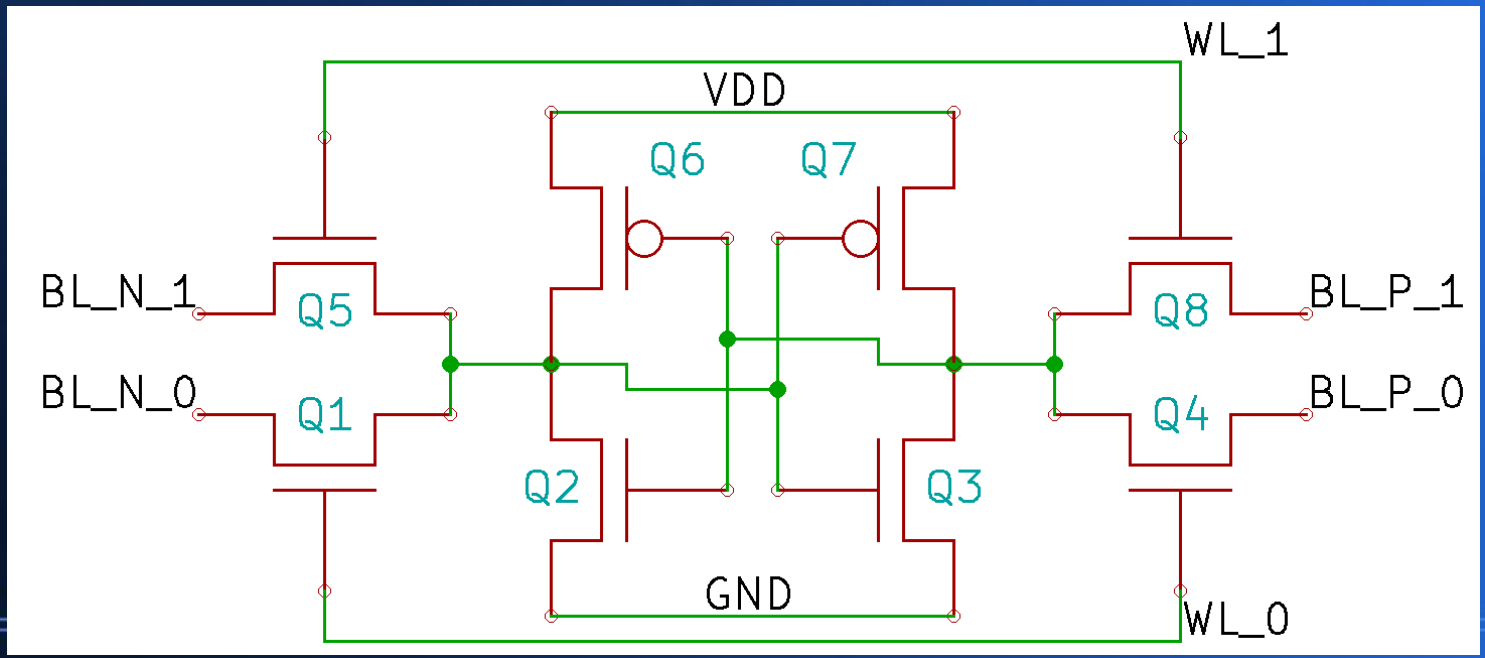
- 4 NMOS transistors, 2 resistors
  - The NMOS dual of the 6T CMOS cell
- Denser than 6T, doesn't need separate PMOS
- Harder to manufacture, often slower read times
- Not seen very often in modern processes
  - We've been trying to find an example in the wild for siliconpr0n and haven't seen any

4T SRAM



Multi port RAM

- Allows multiple reads/writes to happen at once
- Several ways to do this
- Most straightforward: Extra access transistors



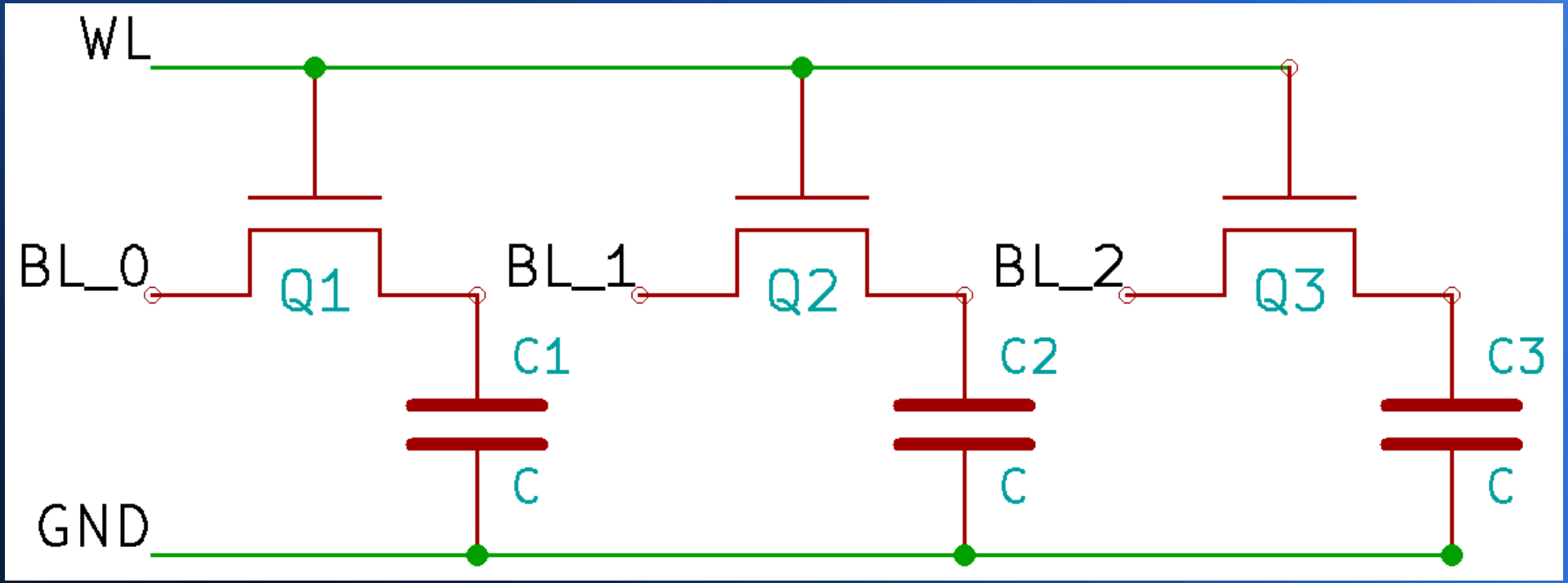
8T cells and more

- Many other cell designs exist
- Most are optimized for higher performance
  - Extra buffering on WLs for reads etc
  - Not seen too often outside high-end SoC/CPU

Dynamic RAM (DRAM)

- Basic cell is a capacitor and access transistor
- Very dense (1T/1C)
- Commonly used for PC main memory etc, very rarely used on-die (eDRAM)
- Charge leaks off cap in a few hundred ms, needs constant refreshing

DRAM schematic



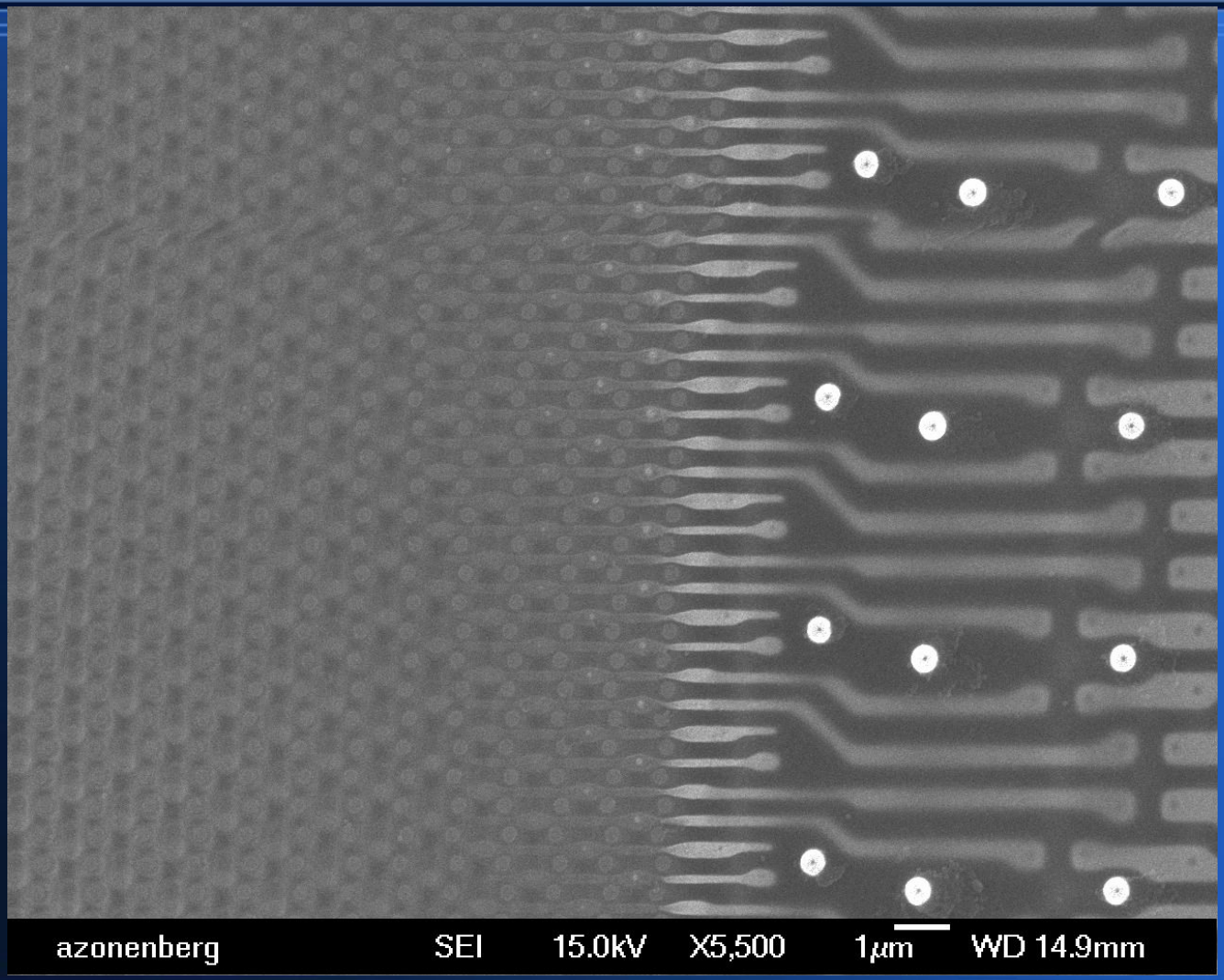
DRAM operation

- Read
  - Precharge bit lines
  - Activate row
  - BLs for 0 bits go low, BLs for 1 bits stay highish
  - Read is destructive, cells are now all zero

DRAM operation

- Write
  - Activate row
  - Drive data onto BLs
  - Close row
- Refresh
  - Read and write same value
  - Refresh one row every few µs round-robin

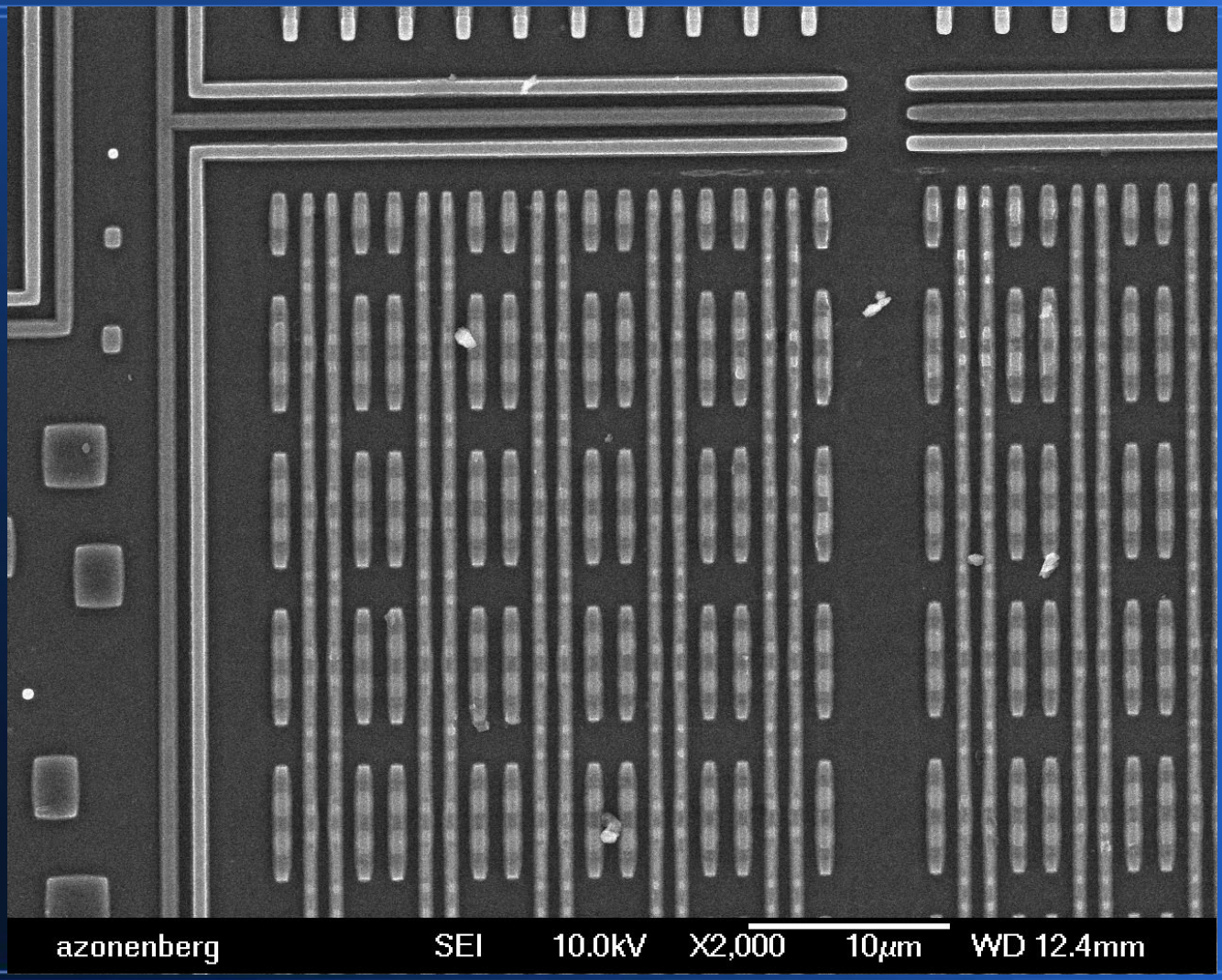
DRAM example



In-class exercise

- Look at some examples of memory and figure out what they are

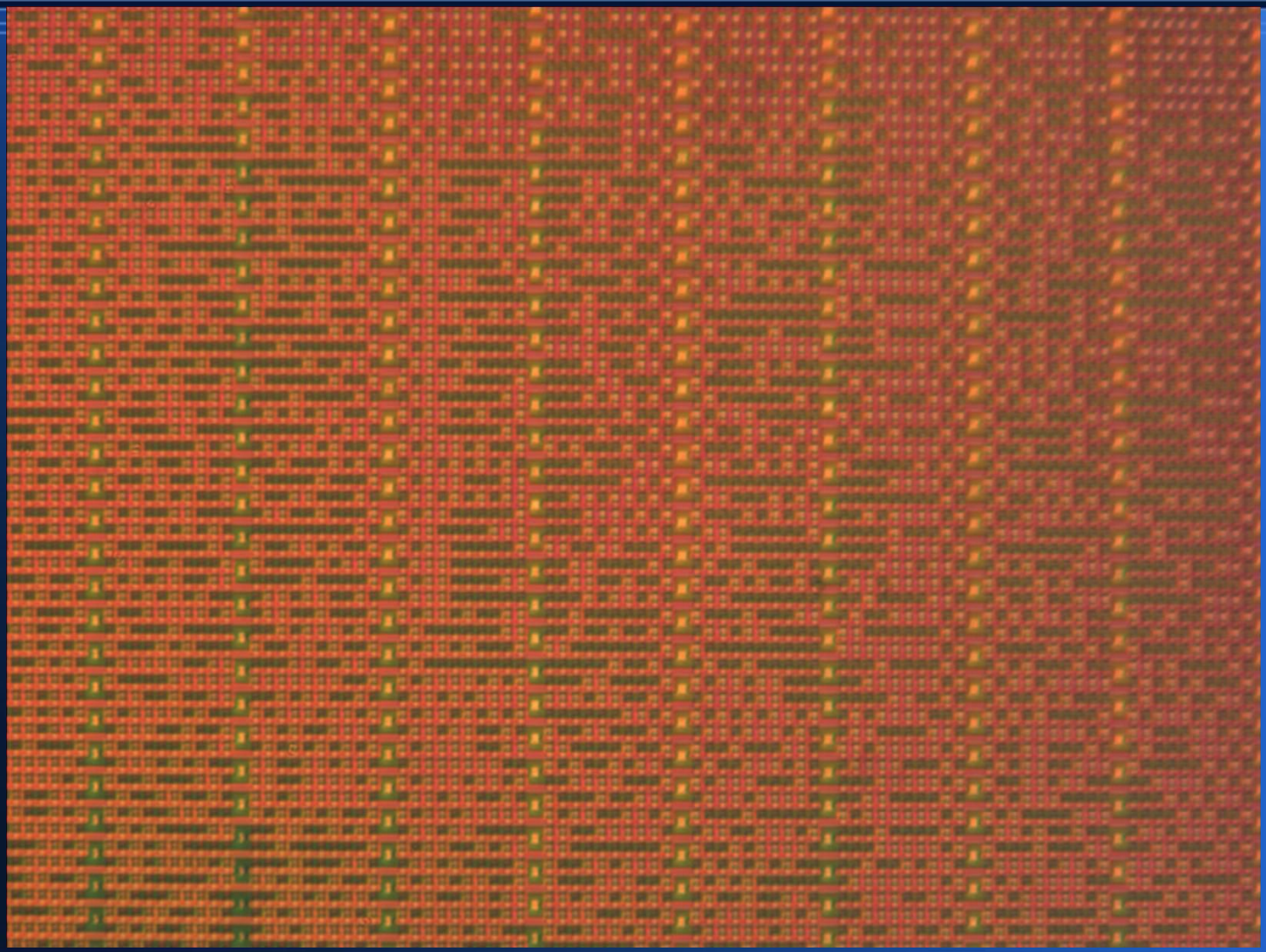
What's this?



2T EEPROM from XC2C32A

- Was initially thought to be NOR flash but closer inspection showed 2T cells, not 1T

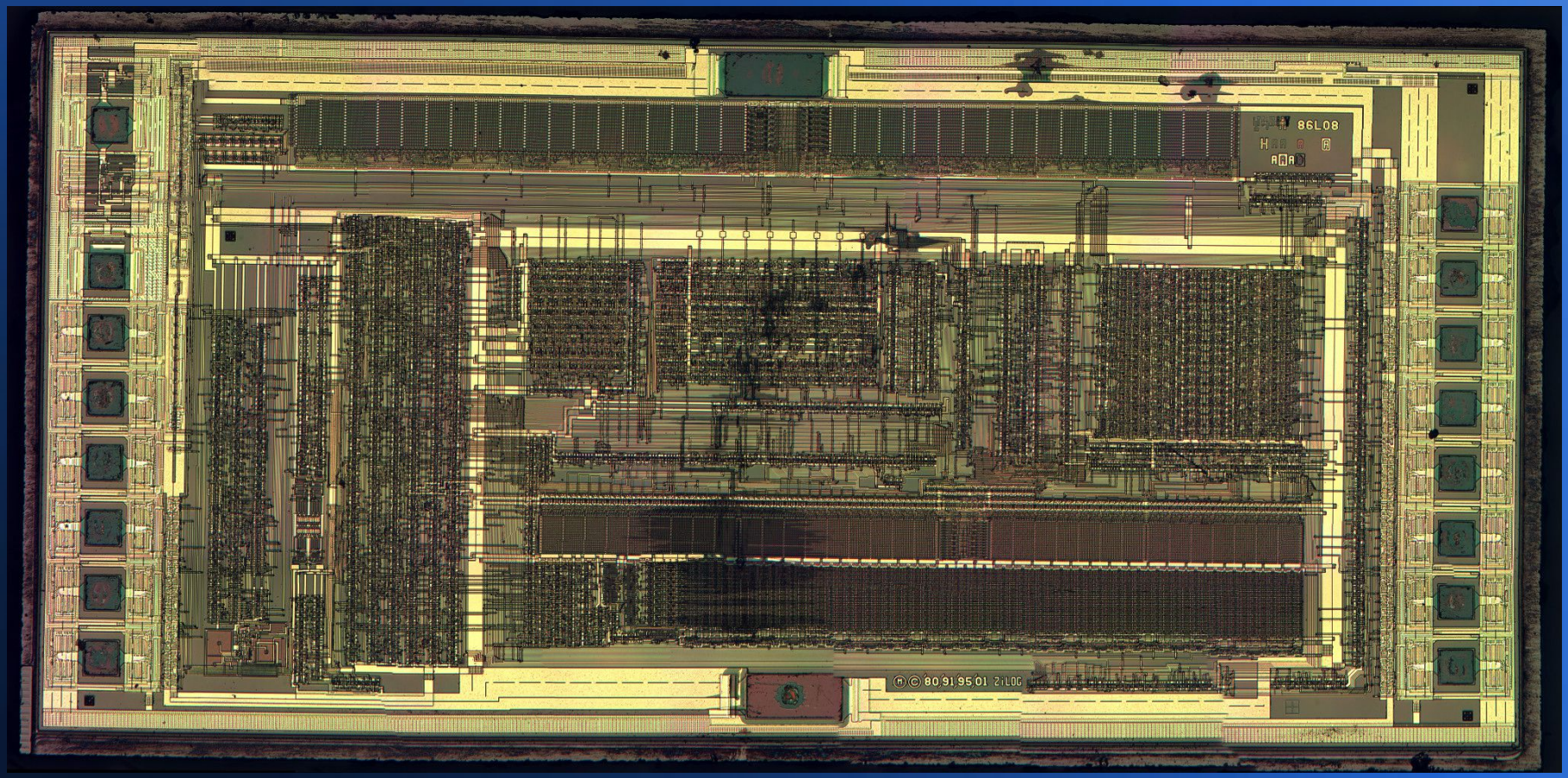
What's this?



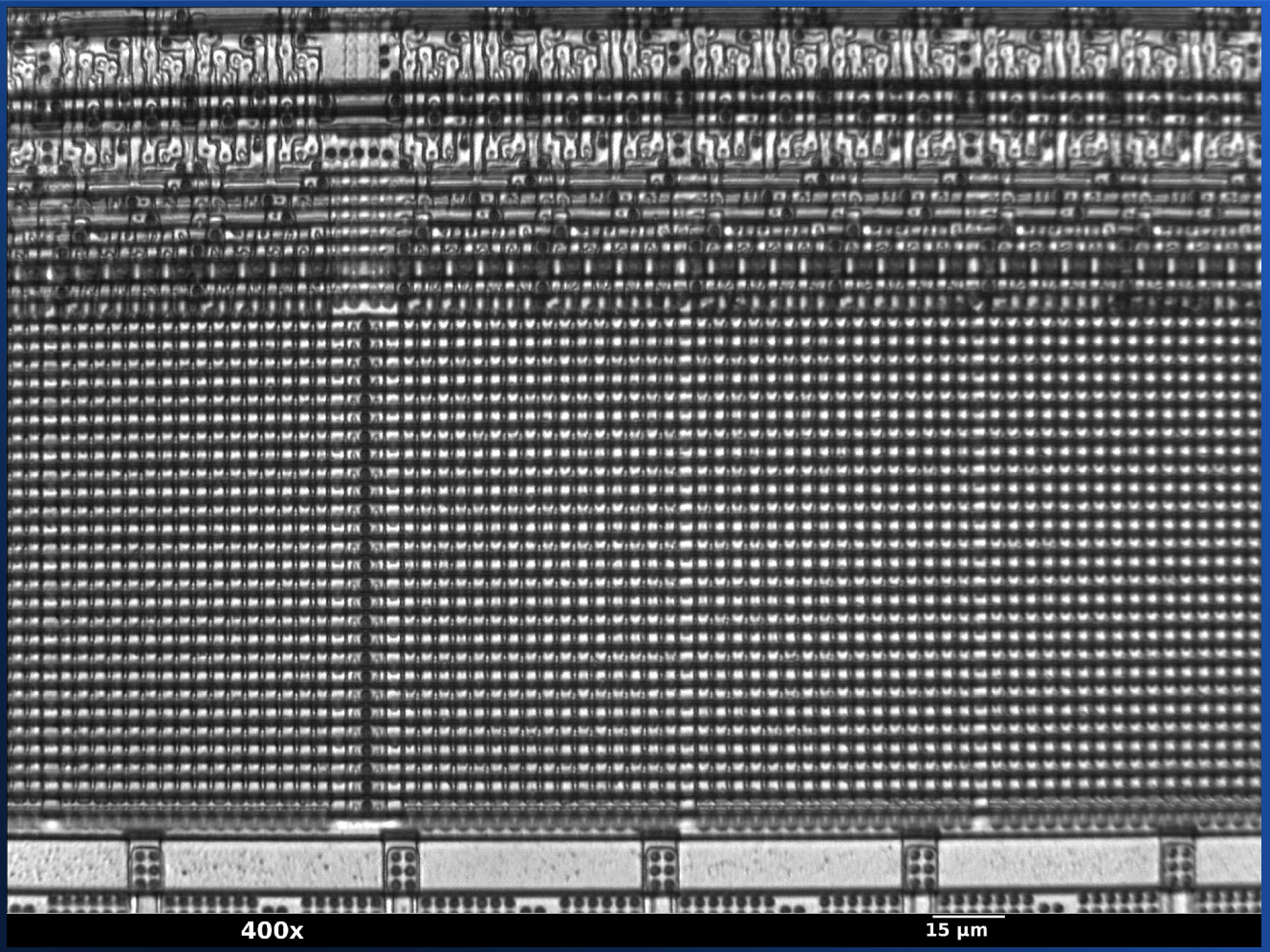
Mask ROM from RSA SecurID 600

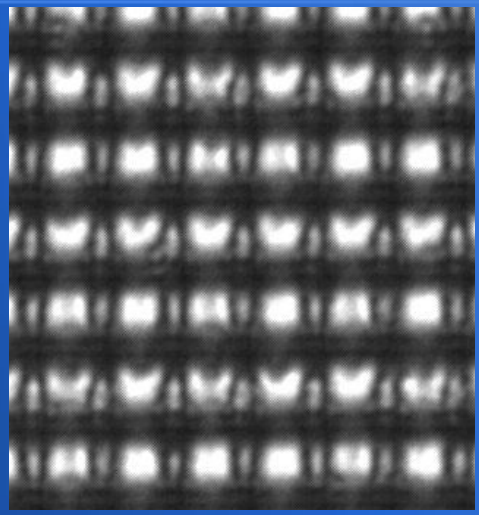
- Appears to be NOR type using contacts
- (not fully dumped yet, some photos are blurry)

Find the memory (Z86L08)



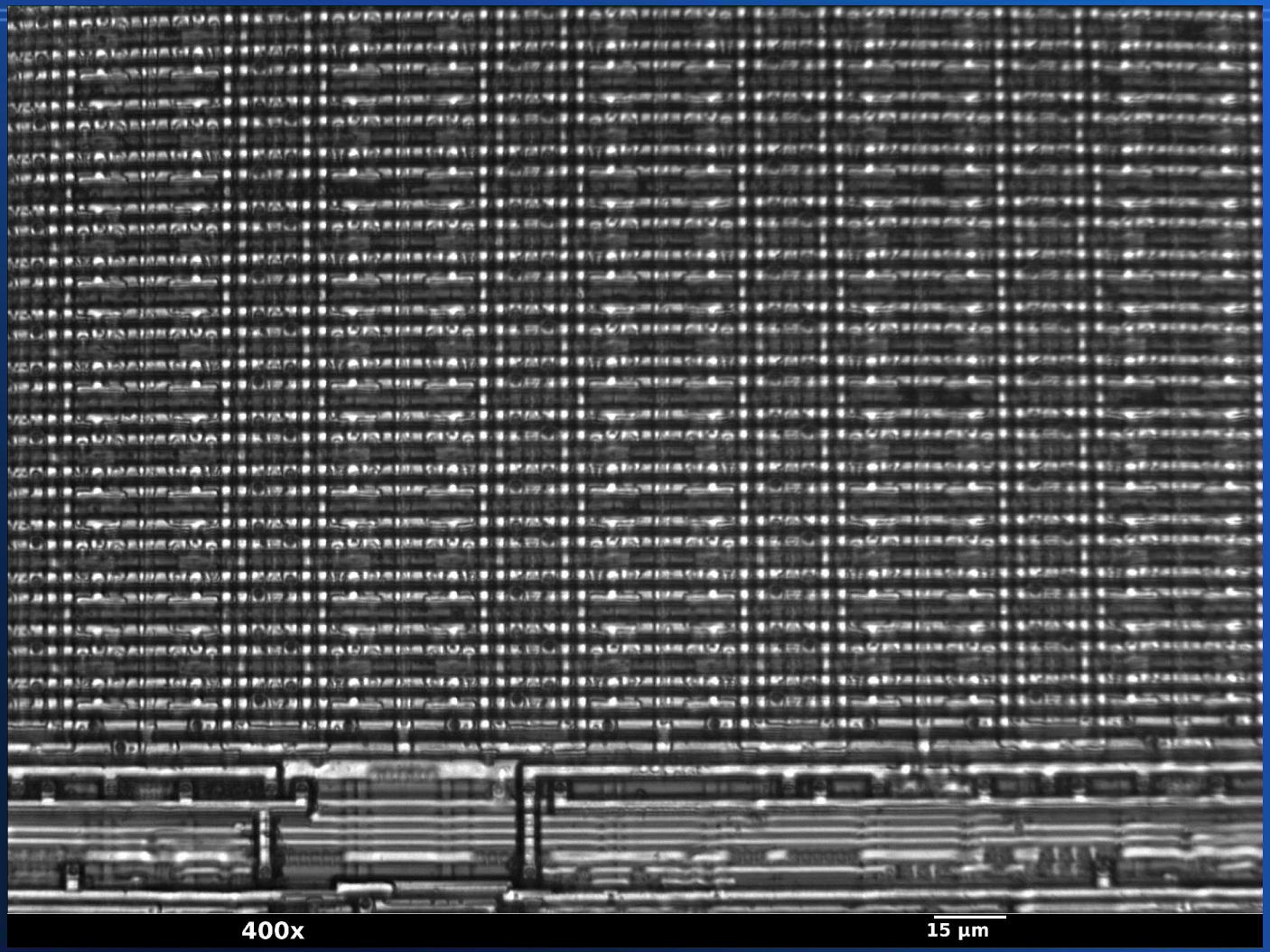
What's this?

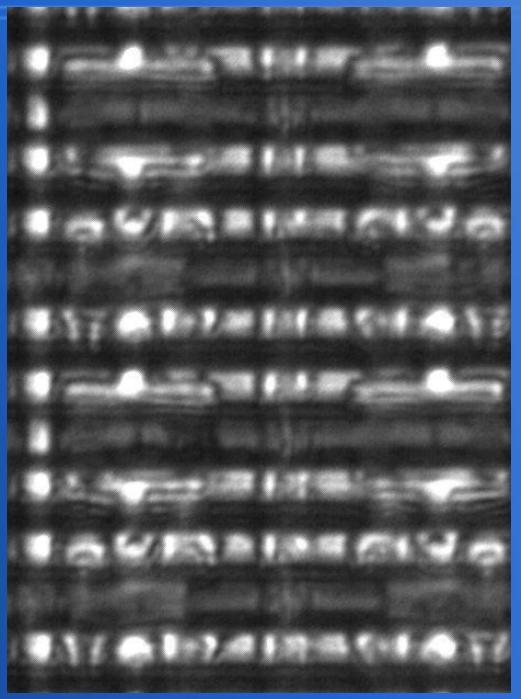




UV EPROM from Z86L08

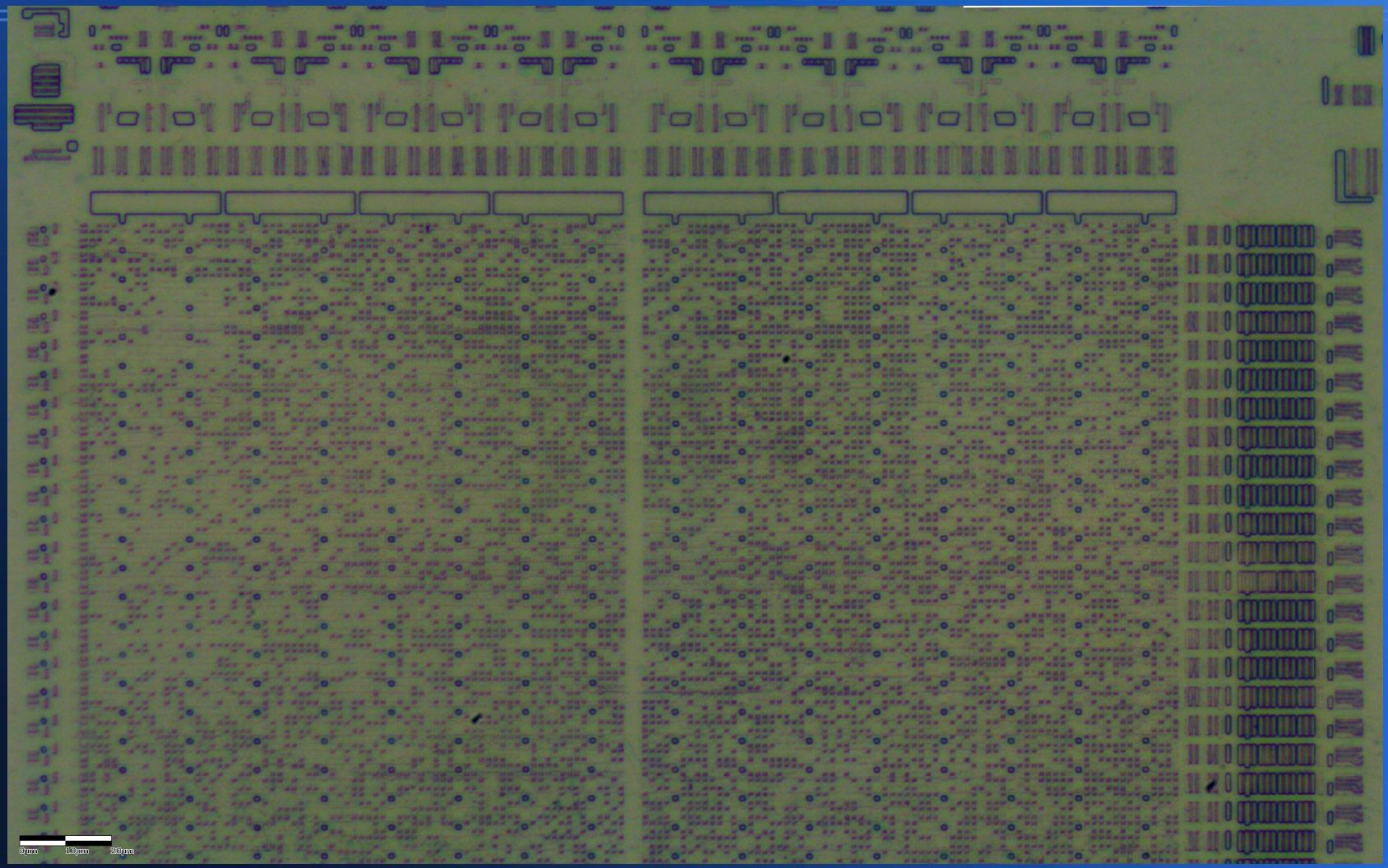
What's this?





SRAM from Z86L08

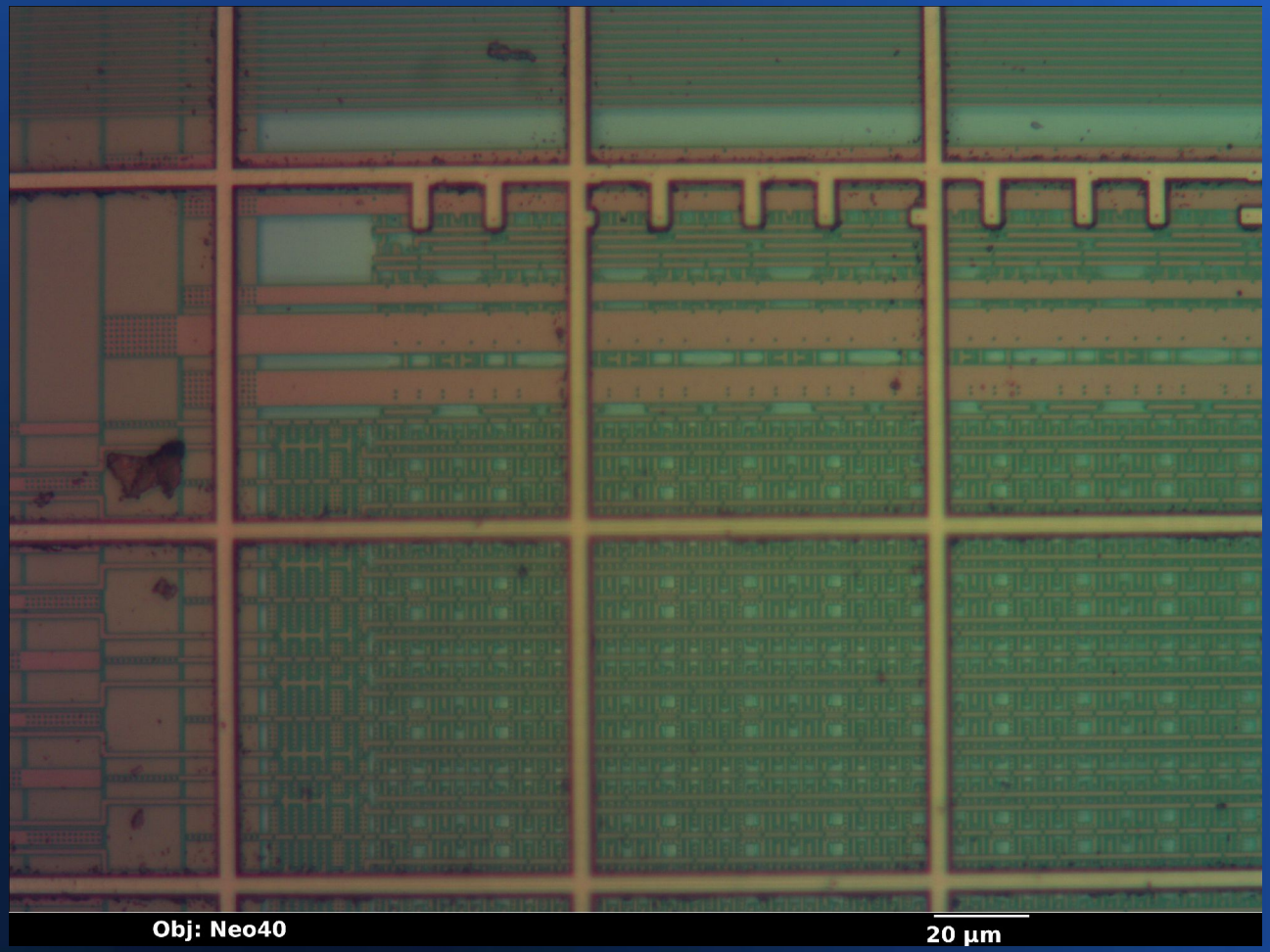
What's this?

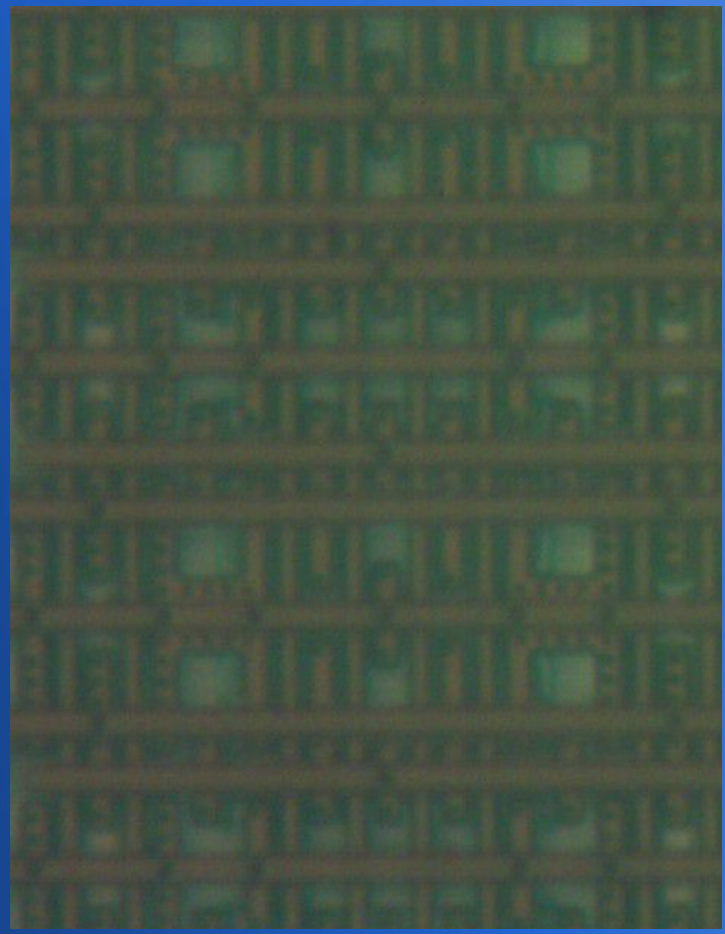


Mask ROM

- From counterfeit FT232RL
  - (Actual die is branded Supereal)
- Hard to tell exact layout from this magnification

What's this?





SRAM from Myricom PCI DMA

Questions?

- TA: Andrew Zonenberg <azonenberg@drawersteak.com>
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